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INSTRUCTION MANUAL
FOR
ME 422A
BIT ERROR MEASURING SET

PREPARED BY

NIPPON ELECTRIC CO., LTD.
TOKYO, JAPAN

PREPARED FOR

HARRIS CORPORATION
ELECTRONIC SYSTEMS DIVISION
MELBOURNE, FLORIDA

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SECTION I

GENERAL

ME422A measuring equipment measures the bit error rate of PCM carrier lines or their associated equipment. The equipment itself consists of transmitting and receiving units. Figure 1-1 illustrates the structure of an entire measuring system.

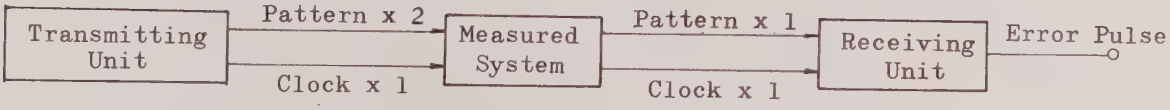


Figure 1-1 Measuring System Structure

The transmitting unit is provided with one route of the clock signal output and two routes of the pattern signal output with 6 bit phase difference between the routes.

The receiving unit is provided with one route for clock signals and pattern signals, respectively, for detecting error pulses. And the error rate is indicated on the meter.

SECTION II

COMPOSITION AND PERFORMANCE

2.1 COMPOSITION

Components of the measuring equipment are listed in Table 2-1 below.

Table 2-1 List of Component

Name	Q'ty	Remarks
ME422A Error Rate Measuring Equipment Transmitting Unit	1	
ME422A Error Rate Measuring Equipment Receiving Unit	1	

2.2 PERFORMANCE

Transmitting unit

(1) Clock frequency

Internal drive: Two frequencies: 1.544 MHz and 7.913 MHz

Deviation: Within $\pm$20 ppm

External drive: 1 MHz - 10 MHz, Sine wave 1 Vp-p, 75 Ω

(2) Pattern signal output

Repetition cycle of false random pattern: (2^6-1) bits

Phase difference between CH1 and CH2: 6 bits

Impedance: 75 Ω

Duty factor: 100%

Level: 0 V/+2 V

(3) Clock signal output

Impedance: 75 Ω

Duty factor: 50%

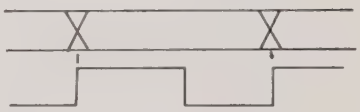
Level: 0 V/+2 V

Rise and fall times: Less than 7 ns

(4) Phase relationship between pattern and clock signal outputs

Pattern signal output

Clock signal output



Phase difference: Within ±5 ns

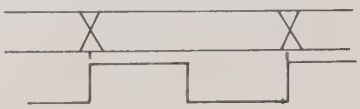
(5) Pattern synchronizing output: Over 0.5 V with 75 Ω load, duty factor 50%

Receiving unit

(1) Phase relationship between pattern and clock signal outputs

Pattern signal output

Clock signal output



Phase difference: Within ±5 ns

(2) Meter indication: Within ±20% with error range 10^{-7}-10^{-8} and error rate 6×10^{-5}

(3) INPUT ALARM: Lighted when either pattern or clock input of both are absent

(4) ERROR: Lighted when error is detected. Lighting time is approximately 50 ms per error pulse.

(5) OVER FLOW: Lights when error rate exceeds 10^{-3}.

(6) Error output: Over 0.5 V with 75 Ω load
Pulse width: Over 20 ns

(7) Recorder output: Over 50 mV with load released.
When error rate is 10^{-3}.

Overall features

(1) When the error rate is measured by directly connecting the transmitting and receiving units, it is below 10^{-10}.

(2) Requirements mentioned above should be satisfied in ambient temperature of 0°C - 40°C and power voltage of 115 V ±10%.

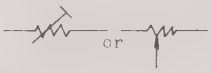
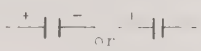
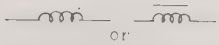
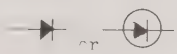
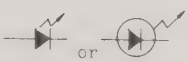
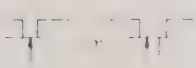
Power Consumption

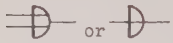
Transmitting Unit	115 V, 50/60 Hz	Less than 50 VA
Receiving Unit	115 V, 50/60 Hz	Less than 50 VA

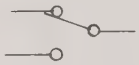
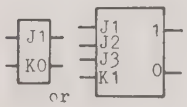
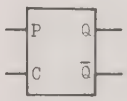
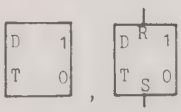
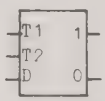
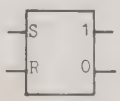
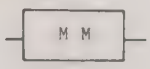
Physical Characteristics

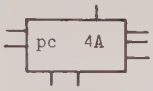
Unit Name	Dimensions						Weight	
	Height		Width		Depth		kg	lb
	mm	inches	mm	inches	mm	inches		
Transmitting Unit	145	5.7	210	8.3	300	11.8	7.5	16.5
Receiving Unit	145	5.7	210	8.3	300	11.8	7.5	16.5

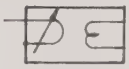
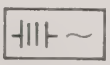
2.3 REFERENCE DESIGNATOR AND CIRCUIT SYMBOL

Circuit Symbol	Reference Designator		Description
	ANRITSU	ASY 32-16	
	R	R	Resistor
	R	R	Resistor, variable
	C	C	Capacitor
	C	C	Capacitor, electrolytic
	C	C	Capacitor, variable
	L	L	Coil
	Q	CR	Diode
	Q	CR	Diode, zener
	Q	CR	Diode, tunnel effect
	Q	CR	Diode, light emitting
	Q	Q	Transistor, NPN
	Q	Q	Transistor, PNP
	Q	Q	Transistor, FET
	X	Y	Crystal

Circuit Symbol	Reference Designator		Description
	ANRITSU	ASY 32-16	
	Q	U	IC, OR-gate
	Q	U	IC, AND-gate
	Q	U	IC, NAND-gate
	Q	U	IC, NOR-gate
	Q	U	IC, Exclusive-or-gate
	V	DS	Lamp
	V	DS	Neon lamp
	T	T	Transformer
	M	M	Timer
	M	M	Meter
		E	Ground connection
		E	Terminal
		P	Male contact
		J	Female contact
		P	Male contact, coaxial
	J	J	Female contact, coaxial

Circuit Symbol	Reference Designator		Description
	ANRITSU	ASY 32-16	
		W	Cable, coaxial
	S	S	Switch
	S	S	Switch, push button
		B	Fan
	J	J	Consent connector, AC power
	Q	U	IC, Flip-Flop, J-K Master-slave
	Q	U	IC, Flip-Flop, J-K master-slave with Preset and Clear
	Q	U	IC, Flip-Flop, D-Type edge-triggered
	Q	U	IC, Flip-Flop, SR-Type
			
	Q	U	IC, monostable multivibrator

Circuit Symbol	Reference Designator		Description
	ANRITSU	ASY 32-16	
	Q	U	IC, operation amplifier
	Q	U	IC, frequency divider
	Q	U	IC in general
	Q	U	IC, current mode logic
			Shift register
			Feedback shift register
			Current mode pulse shaper
		M	Decade counter
			Differenciator
			Memory circuit
			Driver
			BCD-to-Decimal decoder driver
			Level translator
			Schemitt, monostable, multivibrator, wave shaper

Circuit Symbol	Reference Designator		Description
	ANRITSU	ASY 32-16	
			Binary
		AT	Attenuator
		AT	Attenuator, variable
	AT	AT	Attenuator, reactance
		AR	Amplifier
			Emitter follower circuit
			Light emitting diode
			Mixer
			Digital indicator tibe
			Frequency multiplier
		Y	Oscillator
		DC	Directional coupler
	DL	DL	Delay line

SECTION III

PRINCIPLE OF OPERATION

3.1 TRANSMITTING UNIT

Figure 3-1 shows a block diagram of transmitting unit.

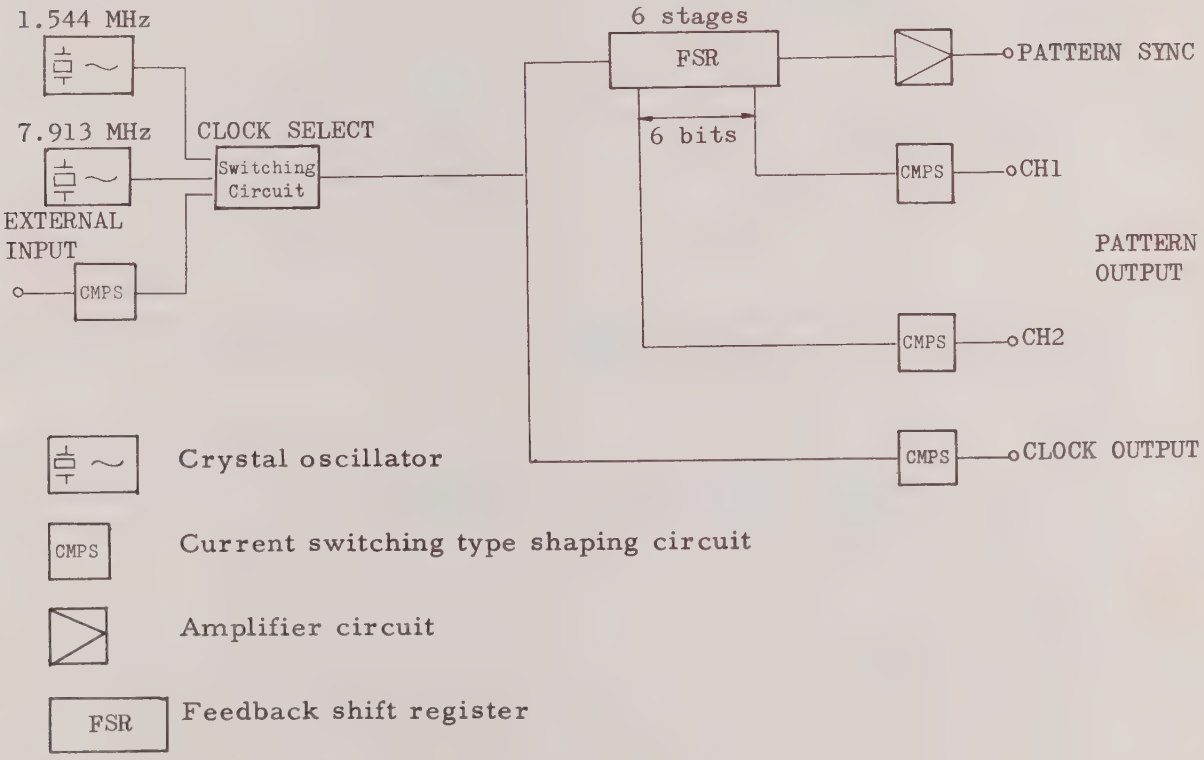


Figure 3-1 Transmitting Unit Block Diagram

The clock signal consists of outputs of two internal oscillators and an external signal. The clock signal selected by the switch out of these three signals is branched into two routes. One goes to the feedback shift register (FSR) circuit, and the other, becomes the clock signal output after passing through the waveform shaping circuit. The clock signal arriving in the FSR circuit drives the 6-stage FSR to generate a false random pattern of 63 bit cycles. Notice in Figure 3-2, that the FSR consists of 6 shift registers and one exclusive OR gate as looped.

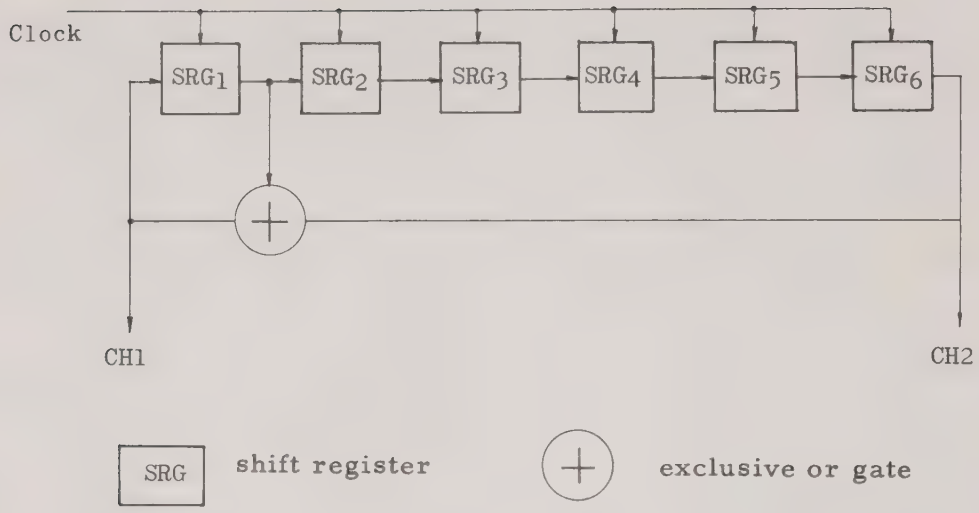


Figure 3-2 FSR Block Diagram

One SRG may be used as a delaying equipment of 1 bit. Therefore the pattern signals of two routes with phase difference of 6 bits may be generated by the 6th SRG as shown in the Figure 3-2.

Pattern signals of two routes from the FSR circuits become the pattern signal output after passing through the waveform shaping circuit. The transmitting unit is also provided with an output for synchronizing the pattern sending out one pulse every 126 bits.

3.2 RECEIVING UNIT

Figure 3-3 is a block diagram of the receiving unit.

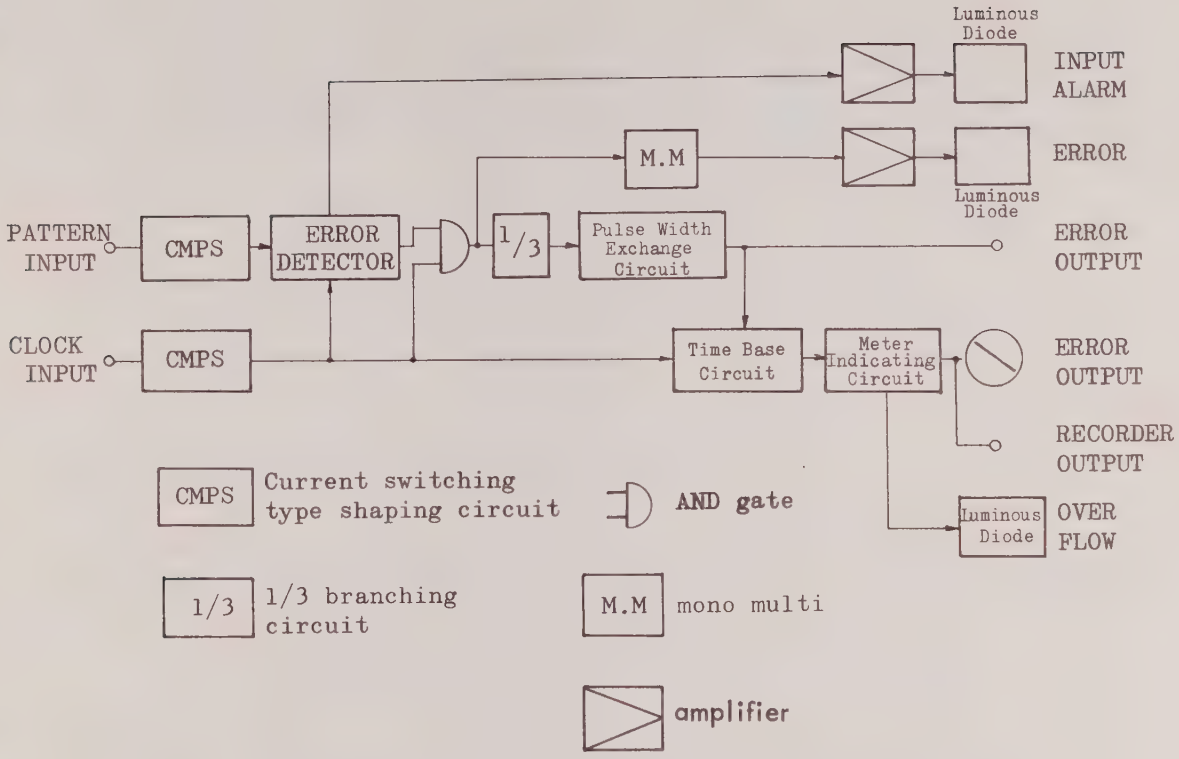


Figure 3-3 Receiving Unit Block Diagram

The receiving unit receives one route of pattern signal and one route of clock signal. Each input signal passes through the waveform shaping circuit to the ERROR DETECTOR circuit.

The block diagram of the ERROR DETECTOR circuit is shown in Figure 3-4.

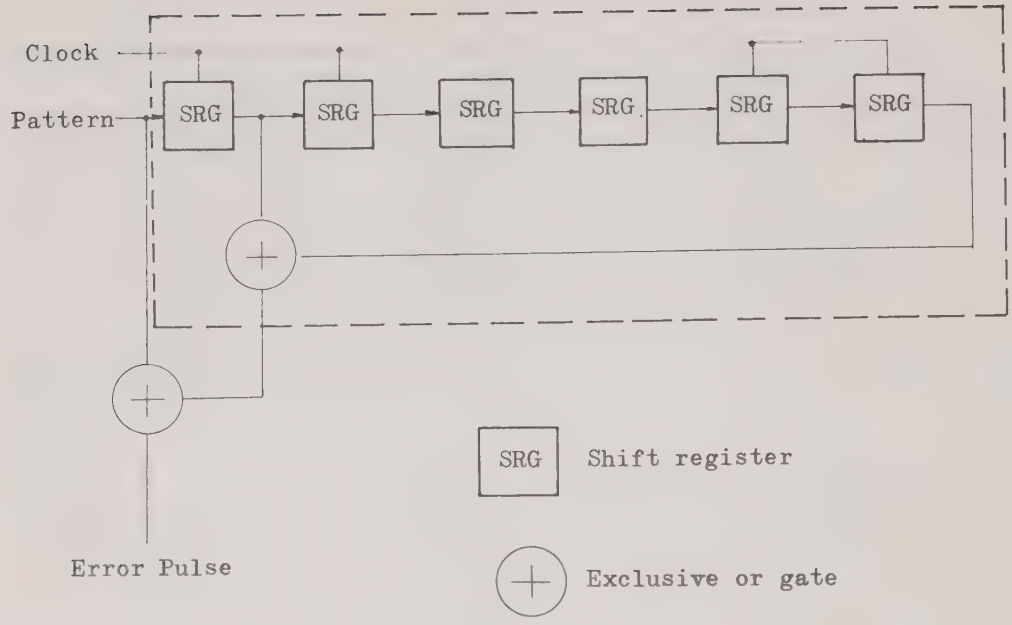


Figure 3-4 Block Diagram of ERROR DETECTOR

The circuitry surrounded by dotted lines is identical to that of the transmitting FSR, except that the input of the first stage shift register comes from an external source, and not from the exclusive or gate.

Therefore, if the output of the transmitting FSR comes in without any change as in the pattern signal, the error pulse will be zero.

If a pulse different from the pattern signal of the transmitting FSR is mixed in the input pattern signal, only the error pulse will be detected by the exclusive or gate. The circuit features multiplication of the number of detected pulses by 3, and also detection of 3 pulses at a time.

These detected pulses, after triggering by the clock signals, are 1/3 fractioned so that one pulse goes out for every error. The input signal, if any, is indicated by the output of SRG in the ERROR DETECTOR circuit. 1/3 fractioned error pulses are branched into 2 routes. One route in passed through the mono multi circuit to make the pulse width approximately 50 ms and thus display the error pulse. The other route is fed to the pulse width converting circuit (width of error pulses becomes approximately 20 ns), and is further branched into 2 routes.

One route becomes the error pulse output and the other route goes to the time base circuit, where clock signals are fractioned to generate 3 kinds of time base signals as shown in Figs. 3-5, (b), (c) and (d). Three kinds of signals, i. e. , AND output of (a) and (b), and (c) and (d) enter the meter display circuit.

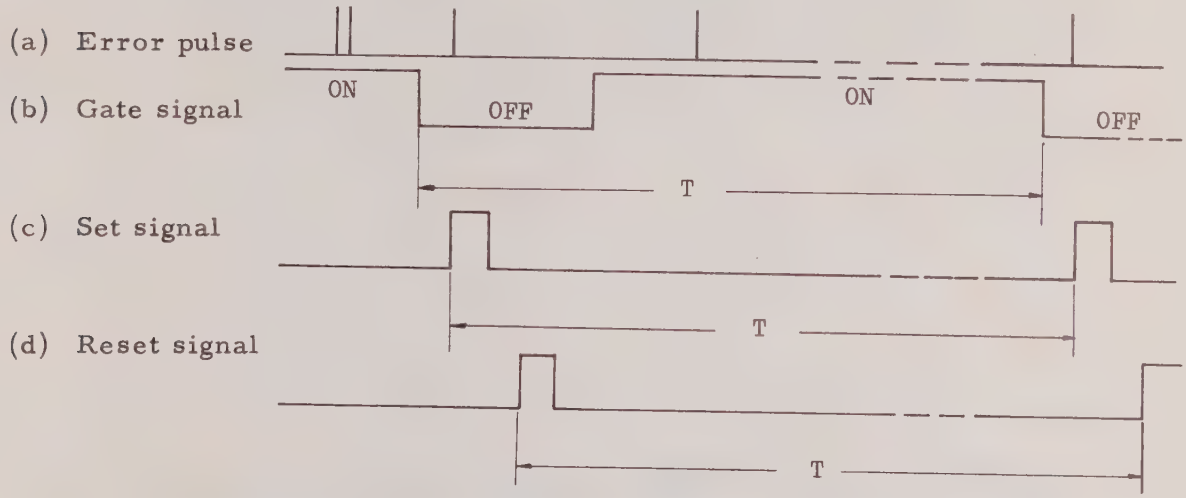


Figure 3-5 Time Relationship between Pulses of the Time Base Circuit

The cycle T of (b), (c) and (d) signals is created by fractioning, the clock signal by 10^7.

A block diagram of the meter display circuit in shown in Figure 3-6.

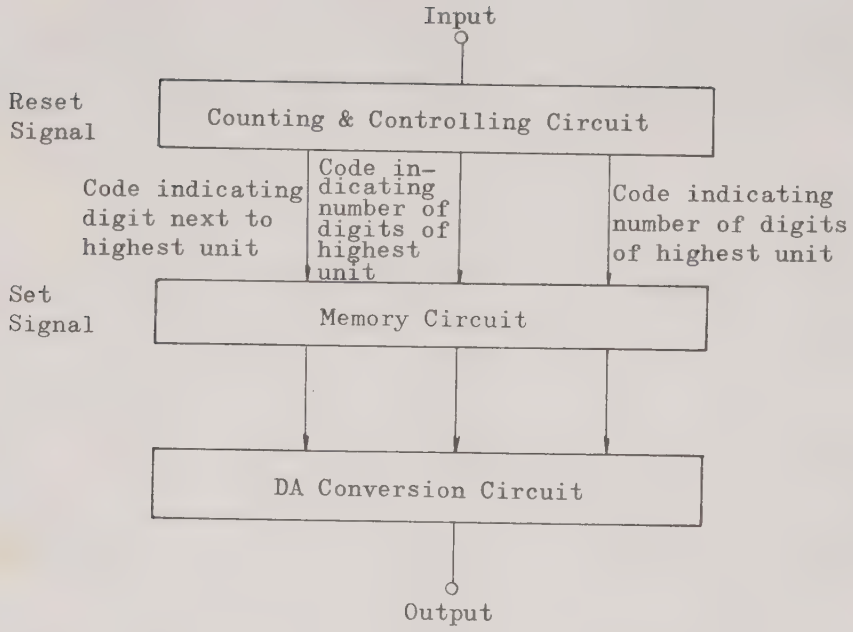


Figure 3-6 Meter Display Circuit Block Diagram

The AND output of the error pulses (discussed above), and the gate signal enter the input. In the counting and controlling circuit, error pulses are counted by a denary counter. Here the figures of the two highest digit numbers and the number of the highest unit are coded.

When the gate signal in Figure 3-5 stops, the denary counter also stops counting and the output signal of the counting and controlling circuit is transferred to the memory circuit by the set signal (Figure 3-5). The output is converted from digital to analog magnitude in the DA conversion circuit. When the memory circuit is set, the counting and controlling circuit reset (with a small time lag), by reset signal shown in the figure. When the gate signal comes in, counting starts in the counting and controlling circuit.

Thus, the same process is repeated. When the meter is driven by the meter display circuit, the signal also becomes the recorder output. The meter display circuit is provided with an output for OVER FLOW to light the lamp when the error rate exceeds 10^{-3}.

SECTION IV

DETAILED DESCRIPTION

4.1 MECHANICAL STRUCTURE

The front, rear, side, top and base covers of this equipment may be pulled off by removing the screws.

For details, refer to Section V.

4.2 DETAILED DESCRIPTION OF ELECTRICAL CIRCUITRY

4.2.1 Transmitting Unit

(1) Clock Circuit (See Drawing 43W13793 in Section VII.)

This circuit is consists two crystal oscillators (Z11, Z12), waveform shaping circuits (Q6, Q7) for external clock signals, and clock signal output circuits (from Q9 to Q14). The external clock signal enters the waveform shaping circuit after passing through the coupling condenser (C10). The clock signal generated here goes into the pattern generating circuit and goes out simultaneously, as the clock signal output after passing through the 2-stage current switching type waveform shaping circuit.

(2) Pattern Generating Circuit (See Drawing 48W3384 in Section VII.)

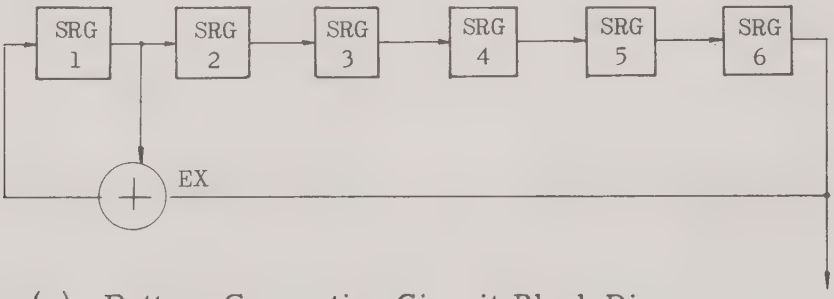
This circuit receives clock signals from the clock circuit and generates false random patterns (from Q1 to Q4) of 63 bits. The pattern repeats a cycle with 1000001111110101011001101110110100100111000101111001010 1000110000. Pattern signals of two routes whose phase difference is 6 bits are generated using the output of the 6th shift register away from the first one (Q2 and Q4). The signals go out as a pattern signal output after passing the two-stage current switching type waveform shaping circuit (from Q15 to Q20 and from Q24 to Q29). There are also, circuits Q6 and Q7 (automatically drive the feedback shift register by detecting its all "0"), and the pattern observing synchronization output circuits from Q6 to Q9 (produce one pulse for every 126 bits of pattern signals). The pattern observing synchronization output sends out the output of Q9 through a coupling condenser (C7).

4. 2. 2 Receiving Unit

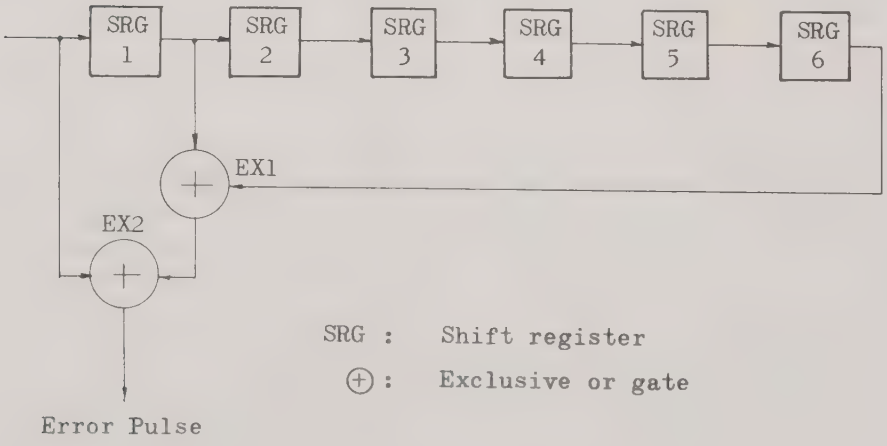
(1) Error Detecting Circuit (See Drawing 48W3387 in Section VII.)

This circuit consists of the pattern signal input, waveform shaping circuits (from Q1 to Q3 and from Q6 to Q8) of the clock signal input, the error detecting circuits (from Q16 to Q19) and the INPUT ALARM circuits (from Q17 to Q24). The waveform shaping circuit consists of an emitter-follower and 1-stage current switching type waveform shaping circuit. The error detecting circuit will be described first.

A block diagram of the pattern generating circuit is shown in Figure 4-1 (a), and that of the error detecting circuit in Figure 4-1 (b).



(a) Pattern Generating Circuit Block Diagram



(b) Error Detecting Circuit Block Diagram

Figure 4-1 Block Diagram

In Figure 4-1 (a), let's assume that the outputs of SRG. 1, SRG. 2 . . . SRG. 6 at a certain time tn are P6, P5 . . . P1, respectively.

The output of SRG. 1 at the time tn + 1 is determined by output P6 of SRG. 1 and P1 of SRG. 6 at the time of tn. Let's assume that it is P7. Then, the following relationship can be established.

$$P7 = P1 + P6 \quad \ldots\ldots \quad (1)$$

+ is an exclusive theoretical total.

As the time passes to tn, tn+1, tn+2 . . . , the output pattern will change to P1, P2 . . . . . P6, P7 . . . . . Let's also assume that these patterns pass through the measured system and come in as P1, P2 . . . . P6, P7 . . . . , and the output of SRG. 1, SPR. 2, . . . SRG. 6 becomes P'6, P'5 . . . . P'1. Since the output of EX1 is the exclusive theoretical total of SGR. 1 and SGR. 6, and P'1 = P1 . . . P'6 = P6 are established on an assumption that no errors occur in P'1 - P'6, the output of EX1 will be equal to P7. If P'7 entering SRG. 1 is normal, i. e. , P'7 = P7, it is equal to the output of EX1 and therefore no error will be detected. If P'7 is not normal, i. e. , P'7 = P7, an error will be detected by EX2. If only P7 is abnormal, the error pulses will be three times, namely, before it enters SRG. 1 (when it becomes the output of SRG. 1 and when it becomes the output of SRG. 6). Therefore there will be 3 error pulses for one error pulse. In case of burst errors, error pulses will be less than three because error pulses off set each other. Circuits of this equipment are designed assuming that 3 pulses will be generated. Detected error pulses enter the succeeding circuit (time base circuit) after being converted into clock signals and AND (Q15). In the INPUT ALARM circuit, the signal for driving the luminuous diode is generated by using the feedback shift register (does not operate unless both pattern and clock signals are present).

The ratio of "1" and "0" of the pattern outputs is almost 1 : 1 as long as the feedback shift register operates. If the register is not operating, the pattern output will become either "1" or "0".

If the pattern outputs are integrated after passing the clamp circuits (from C8 to Q21), the integrated value will vary according to the feedback shift register operation. This change will switch the transistor (Q23) and thus light the luminous diode.

(2) Time Base Circuit (See Drawing 43W13794 in Section VII.)

This circuit receiver error pulses and clock signals (from the error detecting circuit) and generates signals (to light the luminous diode when an error appears), or gate signal for meter indication, or the error output. The error pulse is branched into 2 routes. In one route, it drives the mono multi (Q2) to generate a pulse (width is approximately 50 ms), in order to light the luminous diode and tell the presence of errors. In the other route, error pulses are 1/3 fractioned (Q4), then converted into pulses of approximately 20 ns width. (Q5, Q6) and again branched into 2 routes.

In one route, the pulses become the error output (Q7) and in the other route, they enter the meter indicating circuit afterbeing converted at the gate circuit and AND. The error output consists of a voltage dividing resistor (R7) placed in series with the output of TTL gate (Q7). If a 75 Ω load exists, the level of the error pulse will become approximately 1 Vo-p (zero-to-peak). And if the load is open, the level will become approximately 4. 5 Vo-p.

Clock signals are 10^7 fractioned (Q8 - Q14) so that the error rate can be 10^{-7} when one error pulse is present in one counting cycle. Three kinds of signals shown in Figs. 5-2(a), (b) and (c) (Q15, Q16) are generated out of the 10^7 fractioned signal and the three signals, i. e., AND output of (a) and error pulses, (b) and (c), are sent out to the meter indicating circuit.

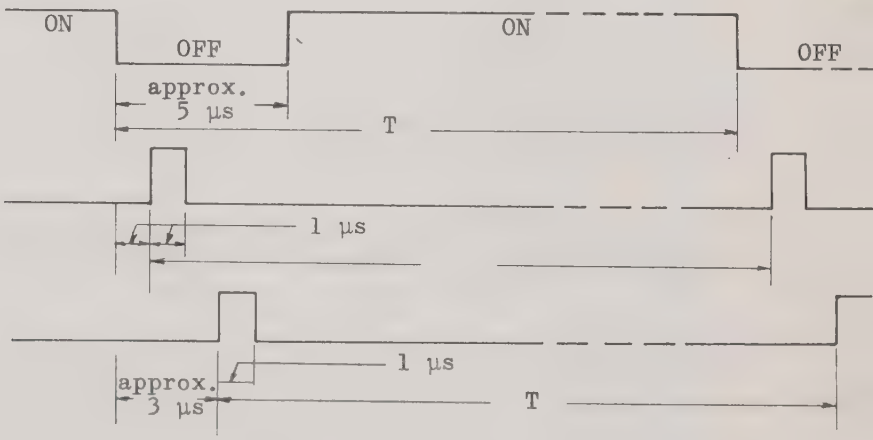


Figure 4-2 Time Base Signal Time Chart

(3) Meter Indicating Circuit (See Drawing 48W3397 in Section VII.)

This circuit counts error pulses to produce signals for meter indication, recorder output and over flow signals.

The portion describing the principle is extracted from Drawing 48W3397 and is indicated in Figure 4-3. The part numbers in Figure 4-3 do not agree to those in Drawing 48W3397. In the following discussion, part numbers in Figure 4-3 are used.

After being converted into overflow signals and AND, error pulses from the time base circuit enter gates Q3, Q4, Q5 and Q6. Let's assume that the 1/10 fractioning circuit (from Q10 to Q13) is preset by the reset signals. Then, only Q6 will be continuous with the controlling circuit, and therefore, the error pulses will enter Q13 via Q6 and Q9 to be counted. The counting value of Q13 is changed from 9 to "0" at the 10th error pulse, whereby the controlling circuit will make Q6 non-countinuous and Q5 continuous. Shortly, thereafter, Q13 will forcibly make "1" in order to memorise digit "1" (second digit of the 10th unit).

If an 11th error pulse comes in, 11 will be indicated by "1" of Q12 and "1" of Q13. From hereon, only the gate of Q5 will remain continuous and error pulses which came in through Q5 will be counted up to 99 by Q12 and Q13.

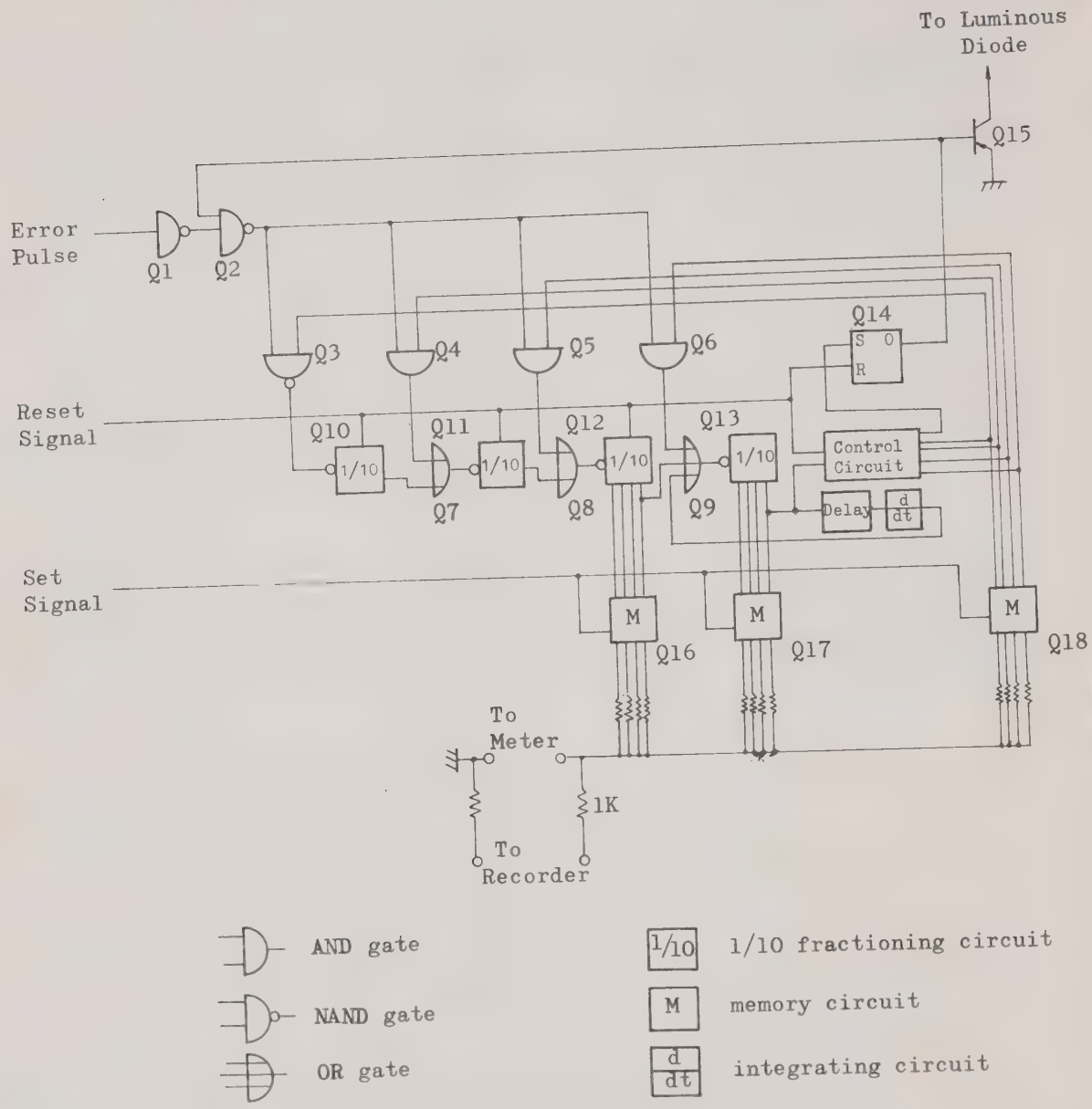


Figure 4-3 Meter Indication Circuit

When the 100th error pulse comes in, Q13 will change to "1" as mentioned above, Q12 will become "0" because the circuit (like Q13), is not provided for Q12. Here, only the gate of Q14 will become continuous, and the fractional circuits of Q11, Q12 and Q13 will be used to count up to 999. When the 100th error pulse comes in, Q13 will become "1", and Q11 and Q12 will become "0", Q3 will become continuous and pulses will be counted up to 9999 by Q10, Q11, Q12 and Q13.

When the 10,000th error pulse comes in, Q14 will operate through change in the control circuit, thus causing gate Q2 to close and the signals for overflow indication to be sent out (Q15). When the gate signal in Figure 4-2 stops, the counted value of error pulses previously counted while the gate signals were ON, will be transferred over to the memory circuits (from Q16 to Q17). As explained above, the error pulses fill up fractional circuits starting from Q13. Therefore the outputs of Q12 and Q13 can always be used to indicate the two highest digits of error pulses. If the number of error pulses is 125, for example, digit 12 is transferred to the memory circuit.

However it indicates only the two highest digit numbers and does not indicate the number of units. A separate circuit Q18 works to indicate the number of units. The number of units is indicated because the number of units of error pulses corresponds to the continuity and non-continuity of Gates Q3, Q4, Q5 and Q6.

After the two highest unit digits and the number of units have been counted separately, they are DA converted by different ladder registers so as to obtain the meter indicating signals.

As soon as the counted value in the 1/10 fractioned circuit has been transferred over to the memory circuit, the denary counter will reset and start counting when the gate signals in Figure 4-2 are ON.

This process is repeated. The control circuit consists of two stage flip flops.

Table 4-1 Control Signal

Number of unit		4	3	2	1
Gate		Q3	Q4	Q5	Q6
Control signal	(a)	0	0	0	1
	(b)	0	0	1	0
	(c)	0	1	0	0
	(d)	1	0	0	0

Gate is continuous when the control signal is "1".

Four kinds of control signals (Table 4-1), are generated by the output of the control circuit, thereby controlling gates Q3, Q4, Q5 and Q6 to indicate the number of units as mentioned above.

When the number of error pulses becomes 10,000, the control signal changes from (d) to (a) to obtain the control signal for overflow.

The internal resistance is less than 65, and the maximum current is 1 mA. The recorder output is less than 65 mA.

4.2.3 Circuits Common to the Transmitting and Receiving Units

(1) Power Source Circuit (Section VII, Drawing 48W3385, 48W3386, 43W13792)

This circuit receives commercial power AC 115 V to generate 5 kinds of stabilized DC power as shown in Table 4-2 below for intra-circuit power supply.

Table 4-2 Power Source

Voltage	Maximum Current Available
-12 V	0.7 A
-5.2 V	1.6 A
-2 V	0.5 A
+5 V	0.8 A
+12 V	0.2 A

AC 115 V power is applied to the primary side of the transformer (T1) via the power filters (L1, L2, C1), fuse (F1) and switch (S1). On the secondary side of the transformer (T1), three kinds of output power are produced, each of which passes through the full-wave rectifier circuits (Q1~Q4, Q5~Q8, Q9~Q12), smoothing capacitors (C2, C3, C4) and series control transistors (Q13, Q14~Q15, Q16), respectively, and enters the printed circuit board of the power source circuit via the mother board. (For the foregoing discussion, see Drawings 48W3385 and 48W3386. For the following discussion, see Drawing 43W13792.)

The three kinds of rectified output power are stabilized in the printed circuit board as follows: The first output power is stabilized at -12 V by the stabilizing IC(Q2). Here, the output voltage is set to -12 V by R3. The second output power is stabilized at -5.2 V by the stabilizing IC(Q9). Here, the output voltage is set to -5.2 V by R8. The third output power is stabilized at +12 V by the stabilizing IC(Q15). Here, the output power is set to +12 V by R13. Power of -2 V is produced from -5.2 V and +5 V power from +12 V by Darlington-connected transistors (Q12~Q13, Q19~Q20). Here, the output power is set to -2 and +5 by R10 and R15, respectively.

SECTION V

HANDLING METHOD

5. 1 DETAILS ON JACKS AND OPERATING BUTTONS AND SWITCHES

5. 1. 1 Transmitting Unit

(Refer to Figs. 5-1 and 5-2, to Table 5-1, and to Drawing 48W3382 in Section VII.)

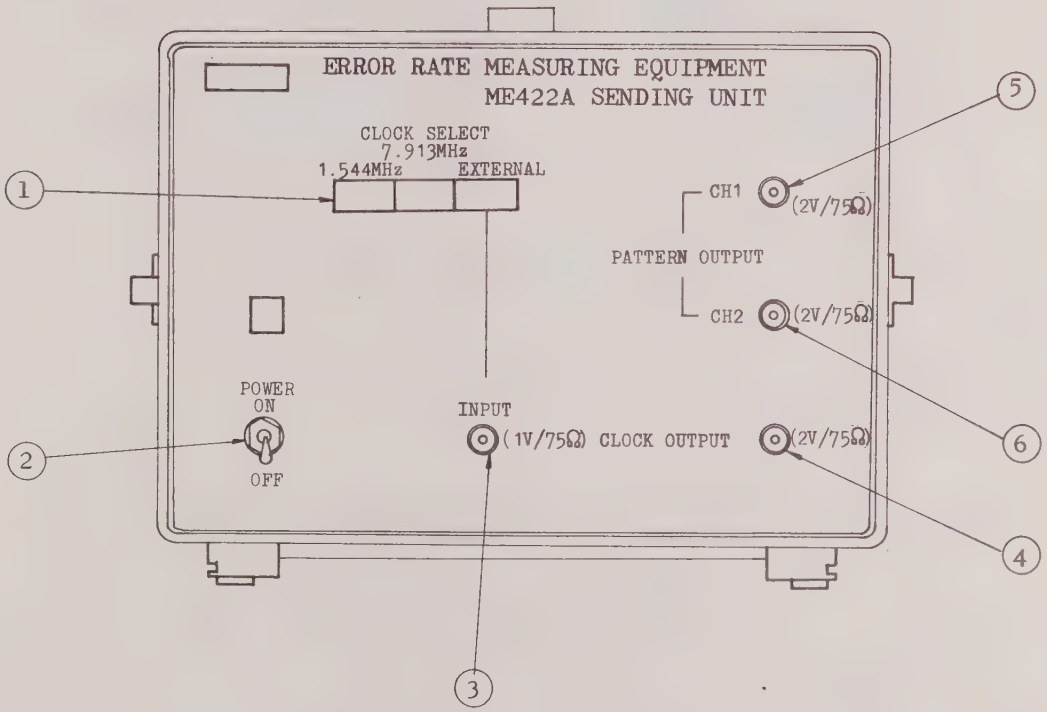


Figure 5-1 Transmitting Unit Front View

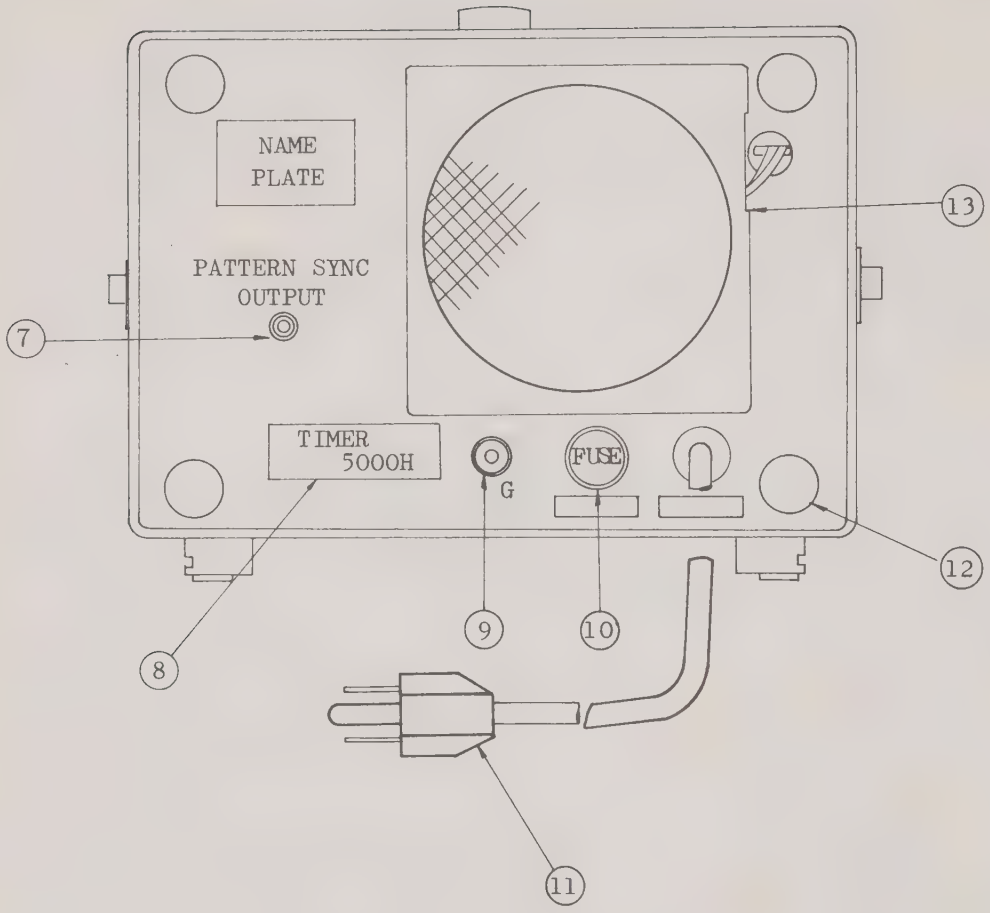


Figure 5-2 Transmitting Unit Rear View

Table 5-1 Controls and Indicators, Transmitting Unit

No.	Nomenclature	Desig.	Function
1	CLOCK SELECT	S2	Switches two waves of internal oscillator and external oscillator.
2	POWER ON OFF	S1	Power switch. Neon lamp light when switch is "ON".
3	INPUT (1 V/75 Ω)	J2	CLOCK peripheral input jack.
4	CLOCK OUTPUT (2 V/75 Ω)	J3	Clock signal output jack.
5	PATTERN OUTPUT	J4	Pattern signal output jacks CH1.
6	CH1 (2 V/75 Ω) CH2 (2 V/75 Ω)	J5	CH2. CH2 retards from CH1 by 6 bits.
7	PATTERN SYNC OUTPUT	J11	Pattern observer synchronizing jack.
8	TIMER 5000H	M1	Measuring equipment Power time meter indicator.
9	G	E1	Grounding terminal
10	FUSE	F1	2A
11		J1	AC 115 V ±10%
12			Power cord winding knob.
13		G1	Cooling fan.

5.1.2 Receiving Unit

Refer to Figs. 5-3 and 5-4, to Table 5-2.

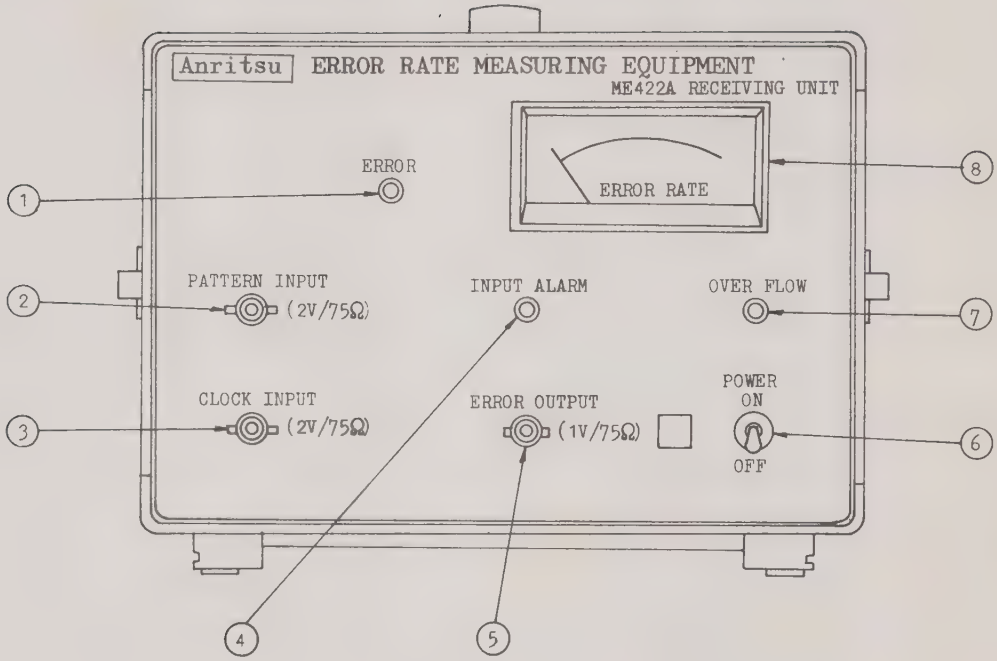


Figure 5-3 Receiving Unit, Front View

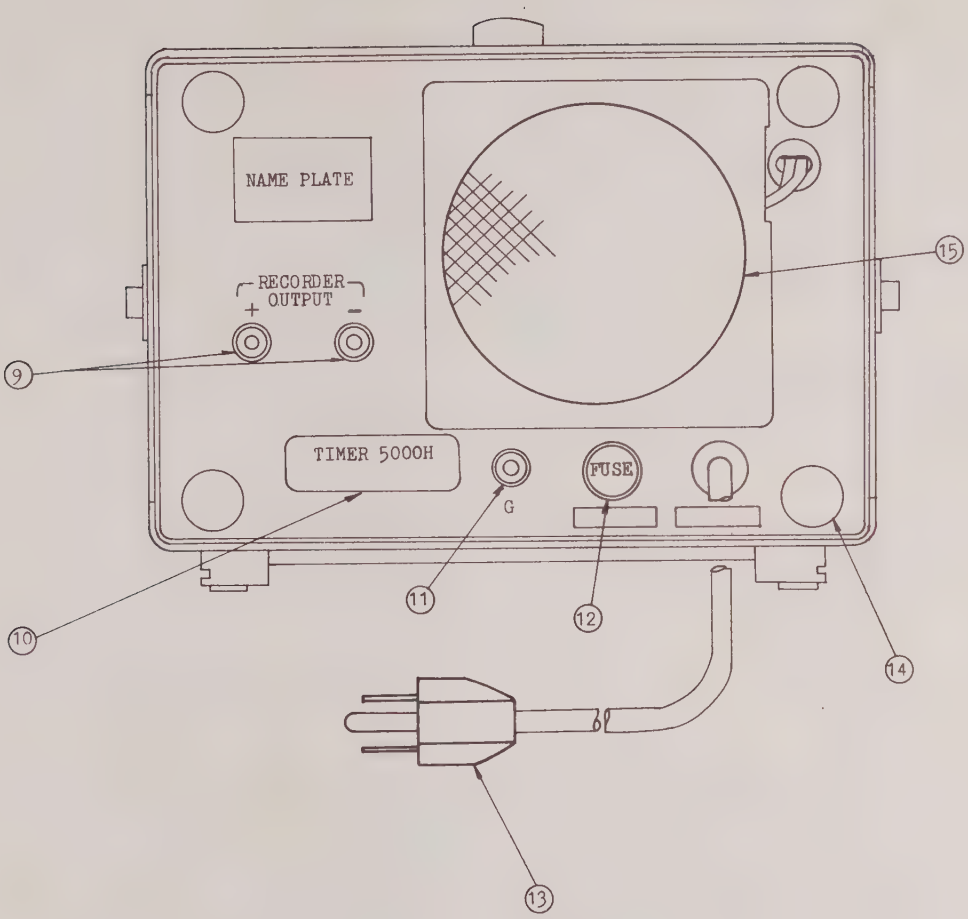


Figure 5-4 Receiving Unit, Rear View

Table 5-2 Controls and Indicators, Receiving Unit

No.	Nomenclature	Desig.	Function
1	ERROR	Q18	Lights when error pulse is detected.
2	PATTERN INPUT (2 V/75 Ω)	J2	Pattern signal input jack.
3	CLOCK INPUT (2 V/75 Ω)	J3	Clock signal input jack.
4	INPUT ALARM	Q17	Lights when either pattern signal and/or clock signal is absent.
5	ERROR OUTPUT (1 V/75 Ω)	J4	Error pulse output jack.
6	POWER ON OFF	S1	Power switch. Neon lamp lights when switch is "ON".
7	OVER FLOW	Q19	Lights when error rate exceeds 10^{-3}.
8	ERROR RATE	M2	Error rate indication meter.
9	RECORDER OUTPUT	E2	Recorder output jack.
10	TIMER 5000H	M1	Measuring equipment power time indication meter.
11	G	E1	Ground terminal.
12	FUSE	F1	2A
13		J1	Power receiving plug, AC 115 V ±10%.
14			Power cord winding knob.
15		G1	Cooling fan.

5. 2 MEASUREMENT

5. 2. 1 Measurement Preparations

1) Connect power cords on rear of transmitting and receiving units to AC115V line and turn on "POWER" switches on front. Lamp on power switch will then light. In the transmitting unit, the clock frequencies are selected by the "CLOCK SELECT" switch. The frequencies can be used for external clock signal (frequency range to 10 MHz) and internal clock signal (frequency 1. 544 MHz, 7. 913 MHz).

2) Connect transmitting unit directly to receiving unit with attached cord. Here either CH1 or CH2 of "PATTERN OUTPUT" on transmitting unit is connected to the receiving unit.

3) Confirm that "INPUT ALARM" and "ERROR" lamps on receiving unit remain unlit in such condition. Needle of "ERROR RATE" meter will not swing either.

Measurement can then be started.

5. 2. 2 Measurement

Connect transmitting and receiving units to measured system with attached cord. If "INPUT ALARM" lamp lights on receiving unit, it means that either pattern or clock signals are not coming in. In such a case, therefore, check the system measured "ERROR" lamp will light if an error occurs in the measured system. As long as only a few errors occur, the lamp will light for every error. As more errors occur, the lamp will remain lig and the needle of "ERROR RATE" meter will start swinging. The needle of the meter will not over-swing if the error rate exceeds 10^{-3} (within range of meter scale), but the "OVER FLOW" lamp will light. The error rate can be read directly on the meter. If the frequency counter is connected to the "ERROR RATE" jack in order to measure the error rate, the following formula may be used, assuming that the frequency indicated on the meter is f.

$$\text{Error rate} = \frac{f}{fc}$$

Here, fc: clock frequency

SECTION VI

MAINTENANCE AND REPAIR

6.1 CALIBRATION

This chapter provides instruction to verify that the ME422A is within the tolerances as specified in paragraph 2.2. Test equipment required for calibration is listed below in Table 6-1. If deviation from standards is noticed with respect to the following items, see paragraph 6.2 "Repair".

6.1.1 Clock Frequency Check

(1) Connect equipment as shown in Figure 6-1.

(2) Press 1.544 MHz switch on ME422A and SEA power switch in ON position on both receiving and transmitting units. Allow 30 minutes warmup period.

(3) Frequency counter will indicate between 1.5437 and 1.5443 MHz. If not, adjust Z11 (shown in Figure 6-26).

(4) Press 7.913 MHz switch on ME422A.

(5) Frequency counter will indicate between 7.91284 and 7.91316 MHz. If not, adjust Z12 (shown in Figure 6-26).

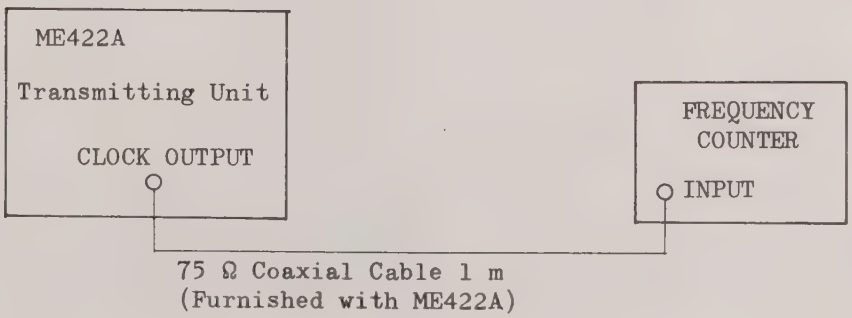


Figure 6-1 Clock Frequency Check

6.1.2 Pattern Signal and Clock Output Check

(1) Connect equipment as shown in Figure 6-2.

(2) Observe the phase difference between channel 1 and channel 2 is as shown in Figure 6-3.

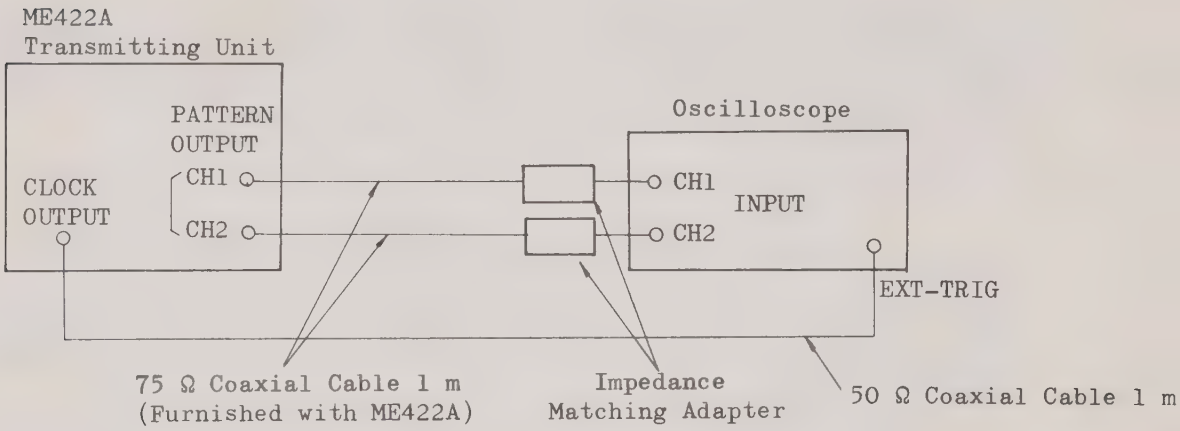


Figure 6-2 Pattern Signal Output Check

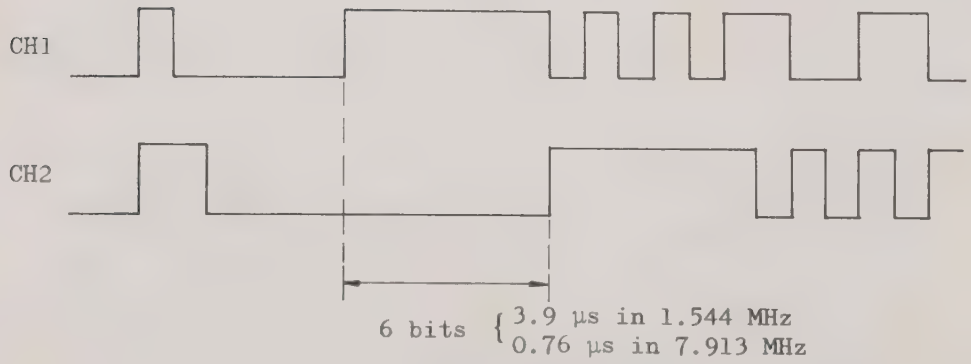


Figure 6-3 Sample Waveform of Phase Relationship

(3) Connect equipment as shown in Figure 6-4.

(4) Observe the leading edge of clock signal is within 5 nsec of the leading edge of the pattern signal output.

(5) The rise and fall time of the clock signal displayed on channel 2 of the oscilloscope will be 7 nsec or less. The output amplitude will be between +1.8 and 2.2 V and between -0.2 and +0.2 V.
(Note: The amplitude must be recomputed if a 75Ω to 50Ω adapter is used.)

(6) The duty factor (symmetry) of the clock signal will be between 45 and 55%.

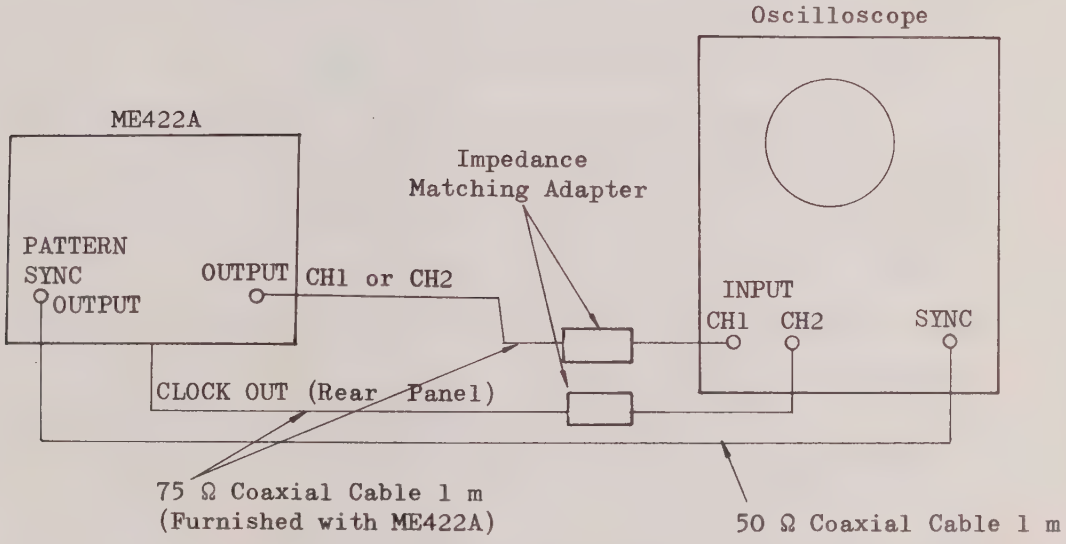


Figure 6-4 Rise-Time Check

6.1.3 Pattern Sync Output Check

(1) Connect equipment as shown in Figure 6-5.

(2) Observe pattern sync output amplitude is at least 0.5 V and duty factor (symmetry) is between 45 and 55%.

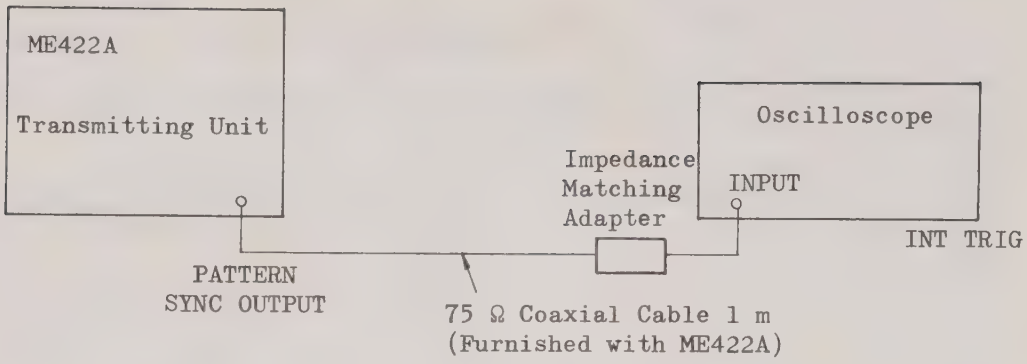


Figure 6-5 Pattern Synchronizing Output Check

6.1.4 Meter Indication Range Check

(1) Connect the transmitting unit channel 1 PATTERN OUT to the receiving unit PATTERN INPUT connector. Use 75 Ω coaxial cable 1 m.

(2) Connect transmitting unit CLOCK OUTPUT to receiving unit CLOCK INPUT. Use 75 Ω coaxial cable 1 m.

(3) Observe that error rate meter on receiving unit indicates 0.

(4) Connect equipment as shown in Figure 6-6.

(5) Set the pulse generator repetition rate to 470 Hz, the pulse width to 126 nsec ±3% and the pulse amplitude to +2 V peak ±10%.

(6) The error rate meter will indicate between 4.8×10^{-5} and 7.2×10^{-5}, and ERROR LAMP glows continuously.

(7) Decrease the pulse generator frequency to 1 Hz. The ERROR RATE lamp will go on and off at a rate of 1 Hz.

(8) Set the pulse generator repetition rate to 8 kHz.
The OVERFLOW lamp will glow continuously.

(9) Disconnect the cable from the receiving unit CLOCK INPUT.
The INPUT ALARM LAMP will glow continuously. Reconnect cable to CLOCK INPUT.

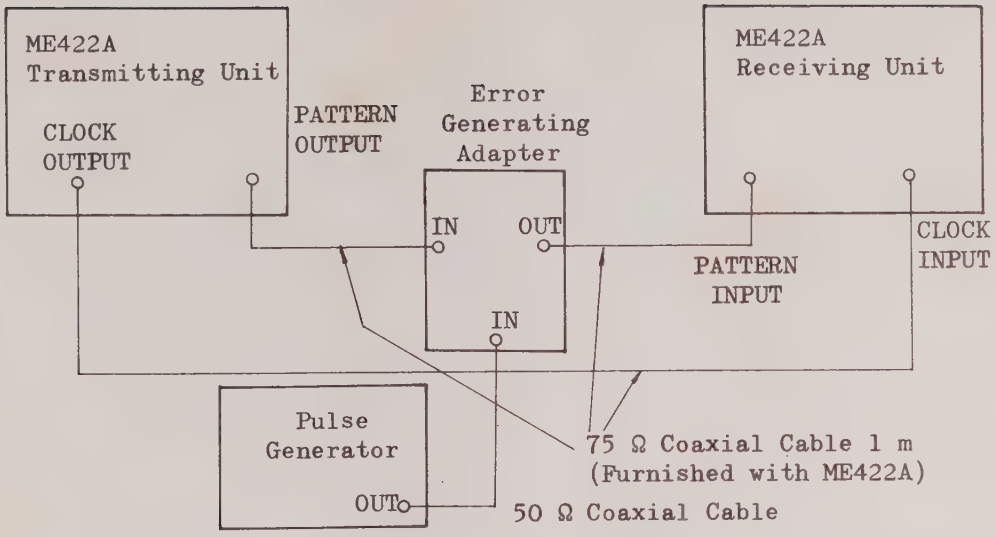


Figure 6-6 Meter Indication Range Check

(10) Disconnect the cable from the receiving unit PATTERN INPUT. The INPUT ALARM LAMP will glow continuously.

(11) Disconnect both cables stated in (9) and (10) above. The INPUT ALARM LAMP will glow continuously.

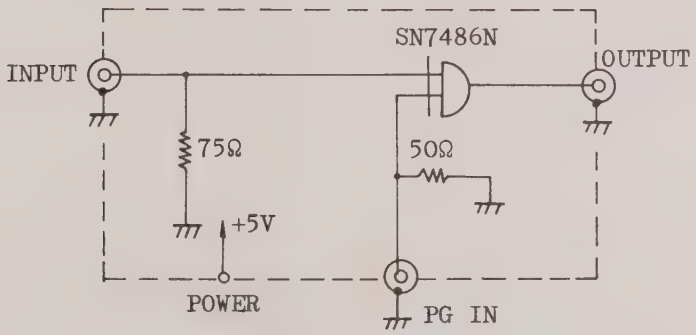


Figure 6-7 Error Generating Adapter

6. 1. 5 List of Equipment for Maintenance and Repair

Table 6-1

Name	Specification	Precautions
FREQUENCY COUNTER	Measuring frequency range: 1. 54 to 7. 92 MHz and 470 Hz Input voltage $\geqq$0. 1 V rms Frequency stability: $\leqq 1 \times 10^{-4}$/day	75 Ω input impedance, in case of measuring cord can be connected directly to COUNTER. In case of 1 MΩ input impedance, use 75 Ω terminator. SYD Model 1037M
OSCILLO-SCOPE	Frequency range: 0 to 50 MHz Sensitivity: 50 mV/cm to 5 V/cm Dual Beam Input impedance: 75 Ω, * $\leqq$ 40 pF or $\geqq$1 MΩ, $\leqq$40 pF	With respect to input impedance, TEK model RM561A with plug-ins 3T77 and 3S1 follow procedures for FREQUENCY COUNTER. * Use 75 Ω to 50 Ω adapter and correct oscilloscope amplitude measurement to compensate for the adapter loss.
PULSE GENERATOR	Frequency range: 1 Hz to 8 kHz Output level: More than 2. 5 V with 50 Ω load. Output pulse width: 126 nsec ±380	H-P 214A or H-P 8403A
CABLE	75 Ω coaxial 1 meter long (Part of ME422A)	
ERROR GENERATING ADAPTER	Shown in Figure 6-7	Item is provided with ME422A for calibration.

6.2 REPAIR

Always pull off power cord first, when checking interior of ME422A Measuring Equipment or when repairing its component.

Remove 16 male screws as in Figure 6-8 to take off lids. Figs. 6-9 thru 6-11 show the transmitting unit and Figs. 6-12 thru 6-14, the receiving unit.

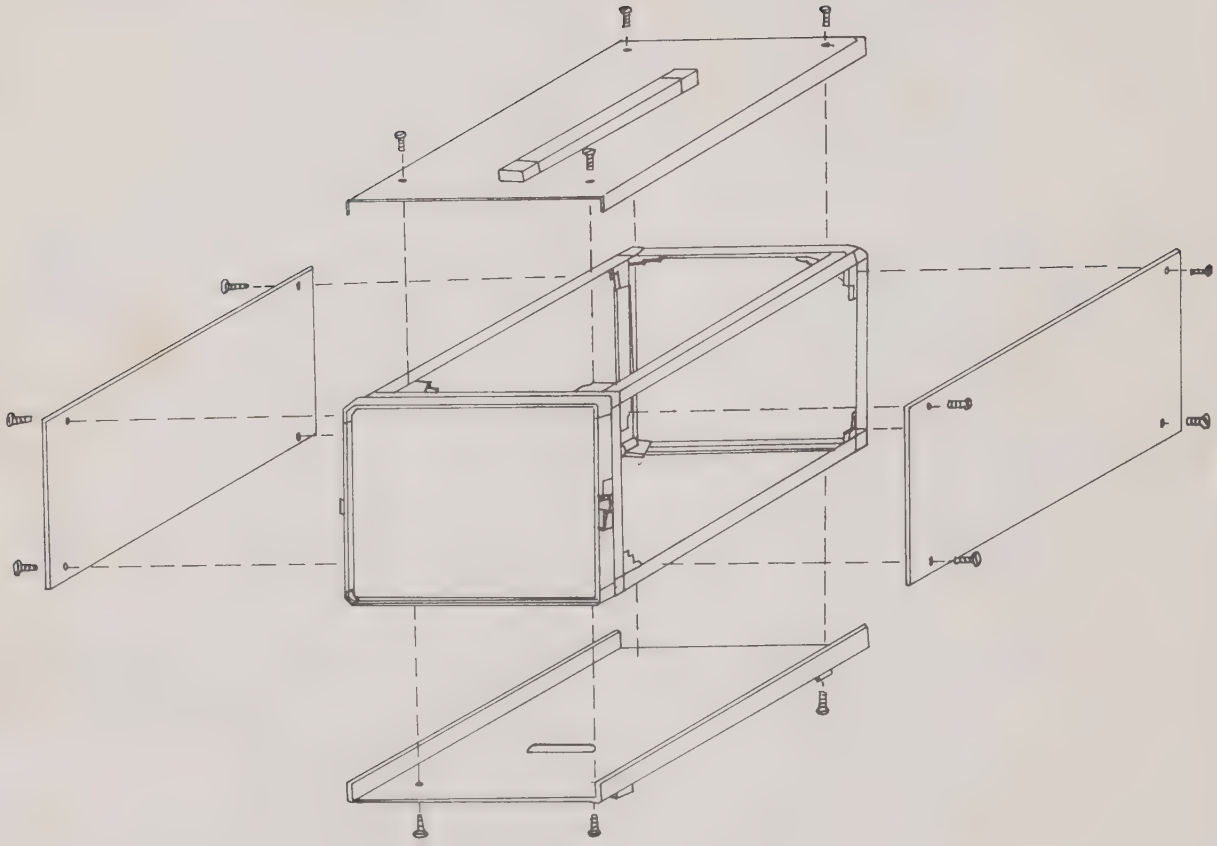


Figure 6-8 How to Take Off Lids

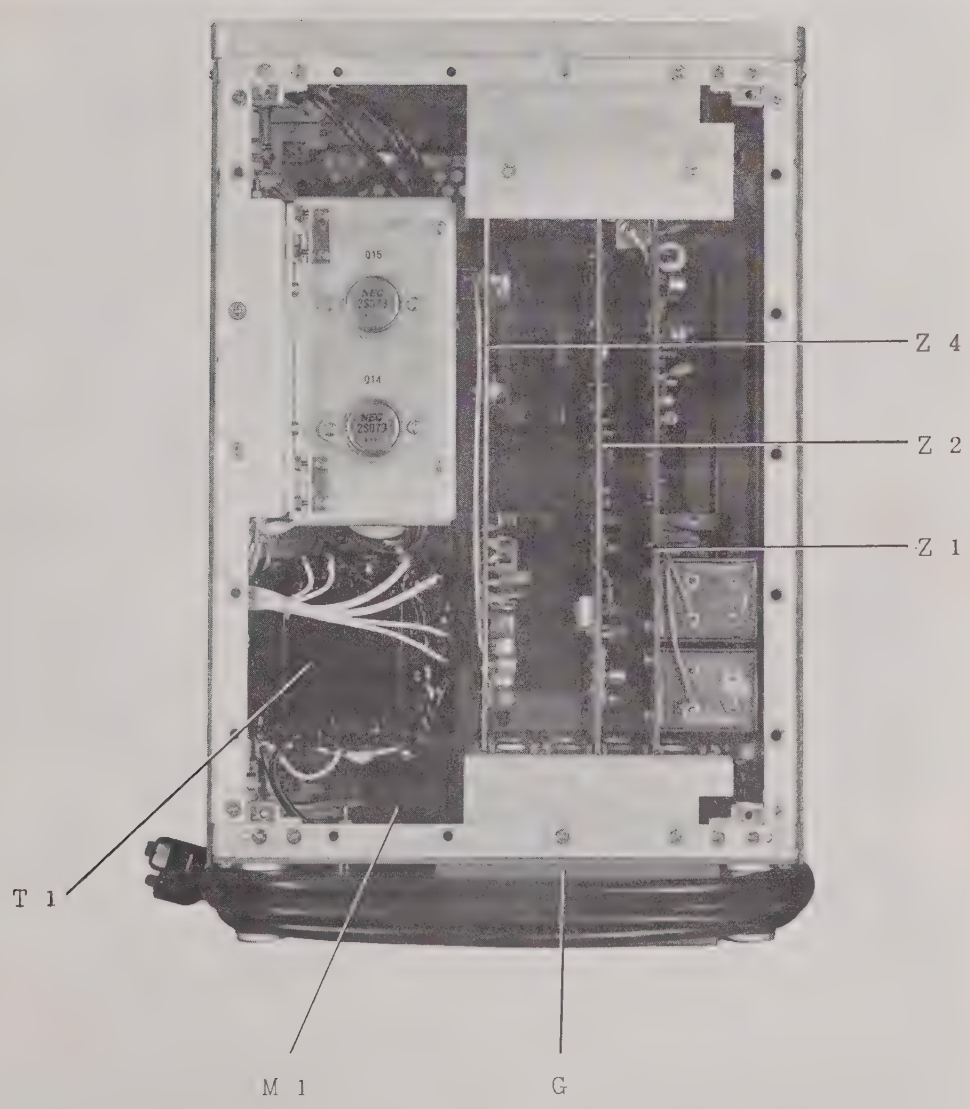


Figure 6-9 Transmitting Unit: Top View

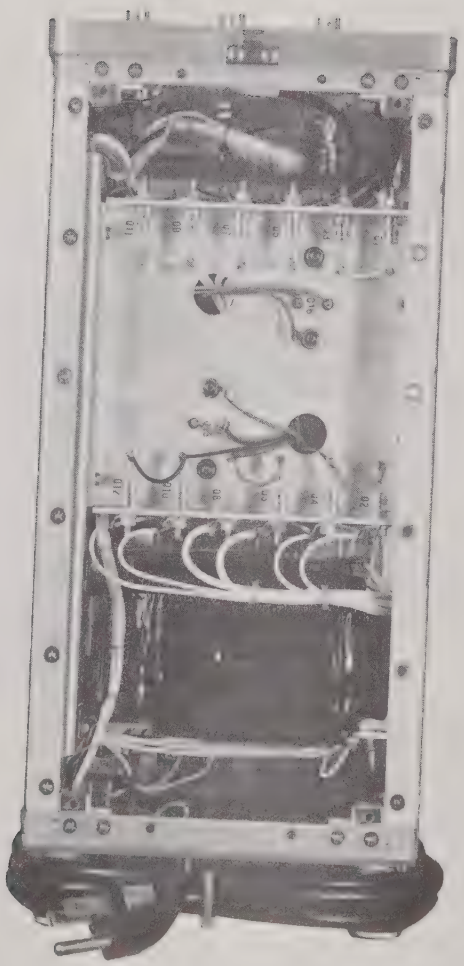


Figure 6-10 Transmitting Unit: Right Side View

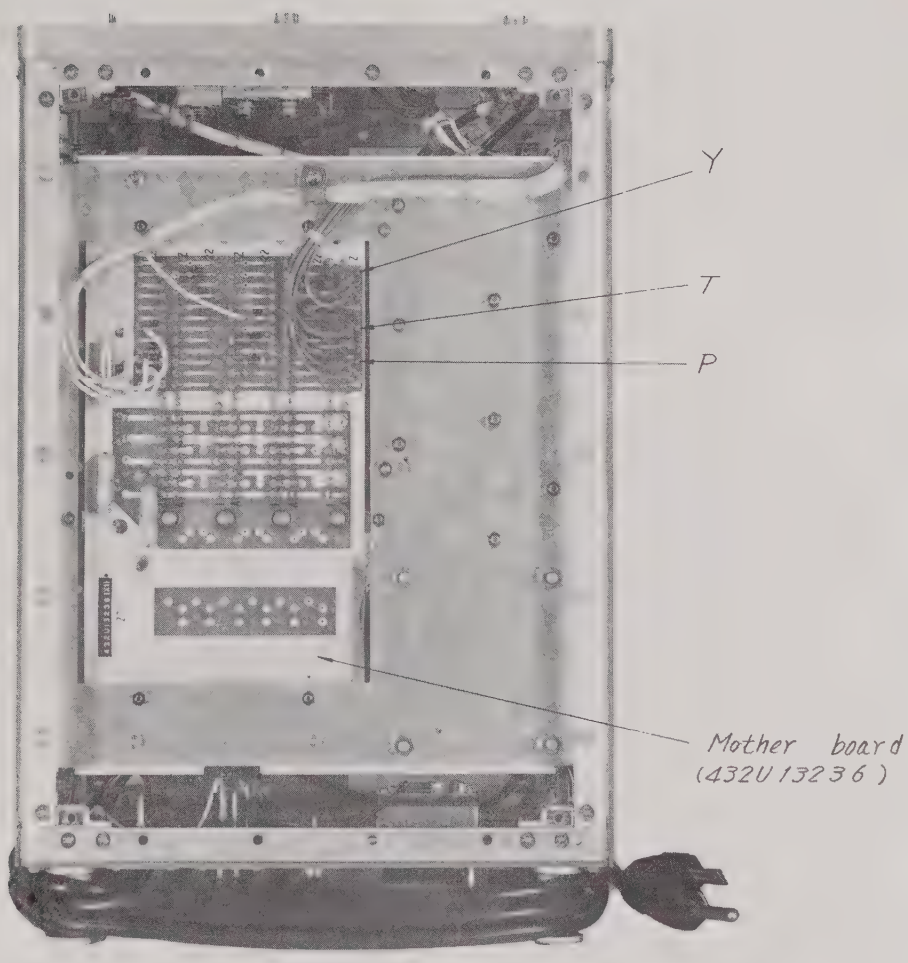


Figure 6-11 Transmitting Unit: Bottom View

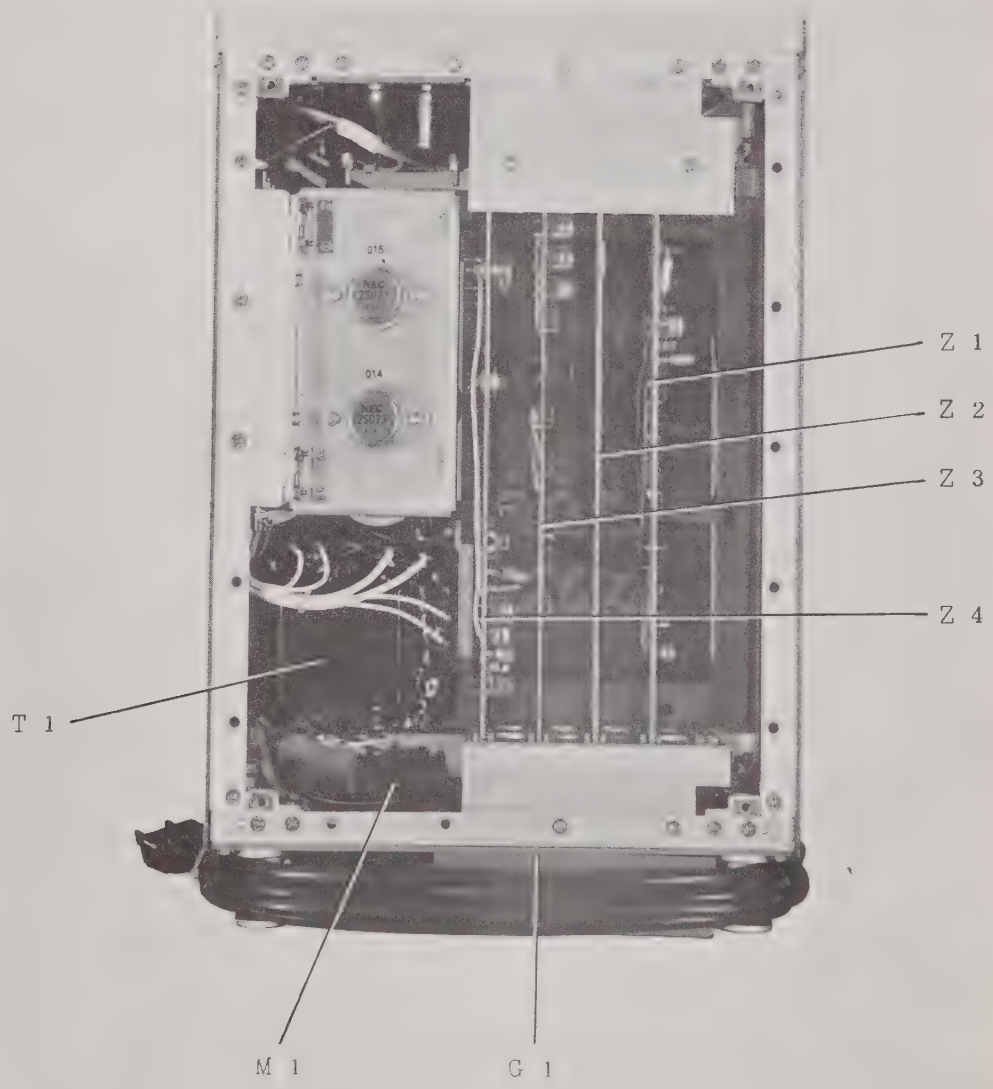


Figure 6-12 Receiving Unit: Top View

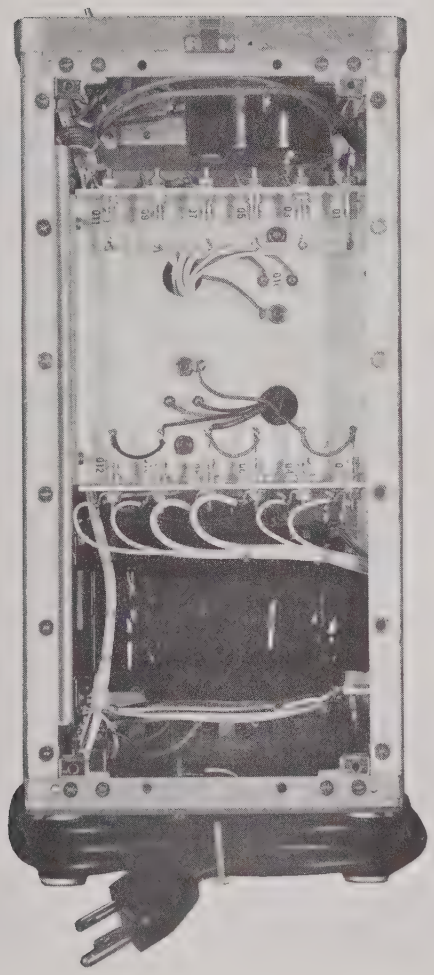


Figure 6-13 Receiving Unit: Right Side View

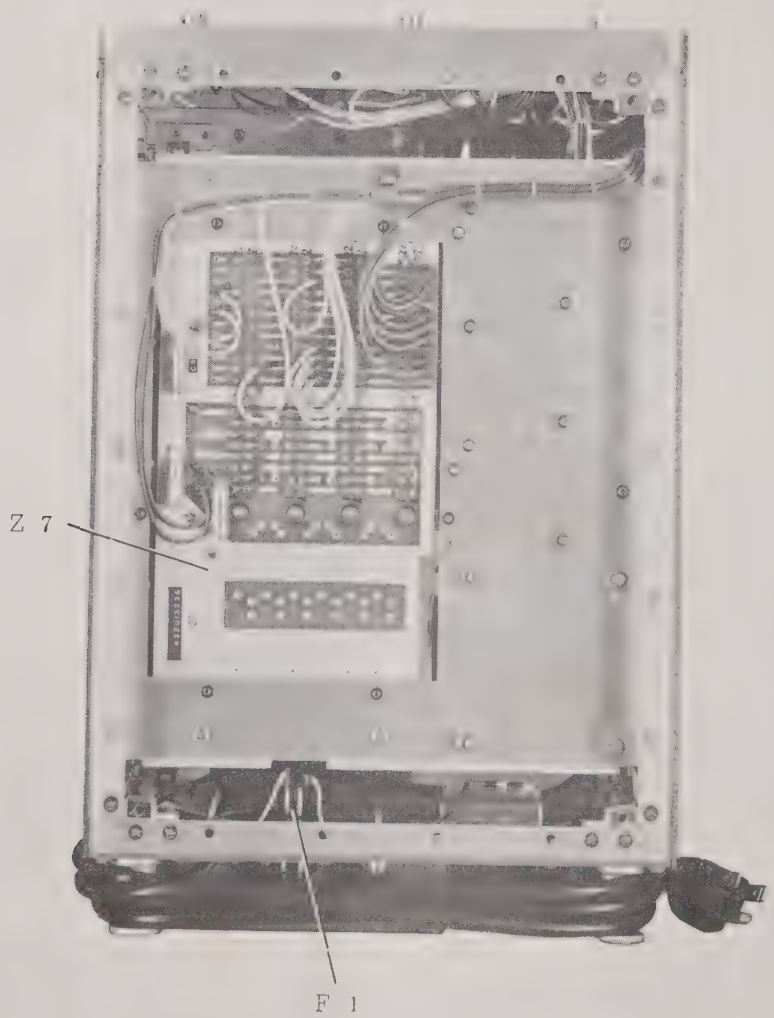


Figure 6-14 Receiving Unit: Bottom View

6.2.1 Power Supply Failure

Check the two items below with respect to -12 V, -5.2 V, -2 V, +5 V, +12 V power supply.

(i) The voltage value indicated shall be within ±5% of specified value.

(ii) The ripple shall be below 0.2 Vp-p.

Figure 6-25 shows the **printboard.**

Voltage values at major points are listed in Table 6-2.

Check item (i) as in Figure 6-15.

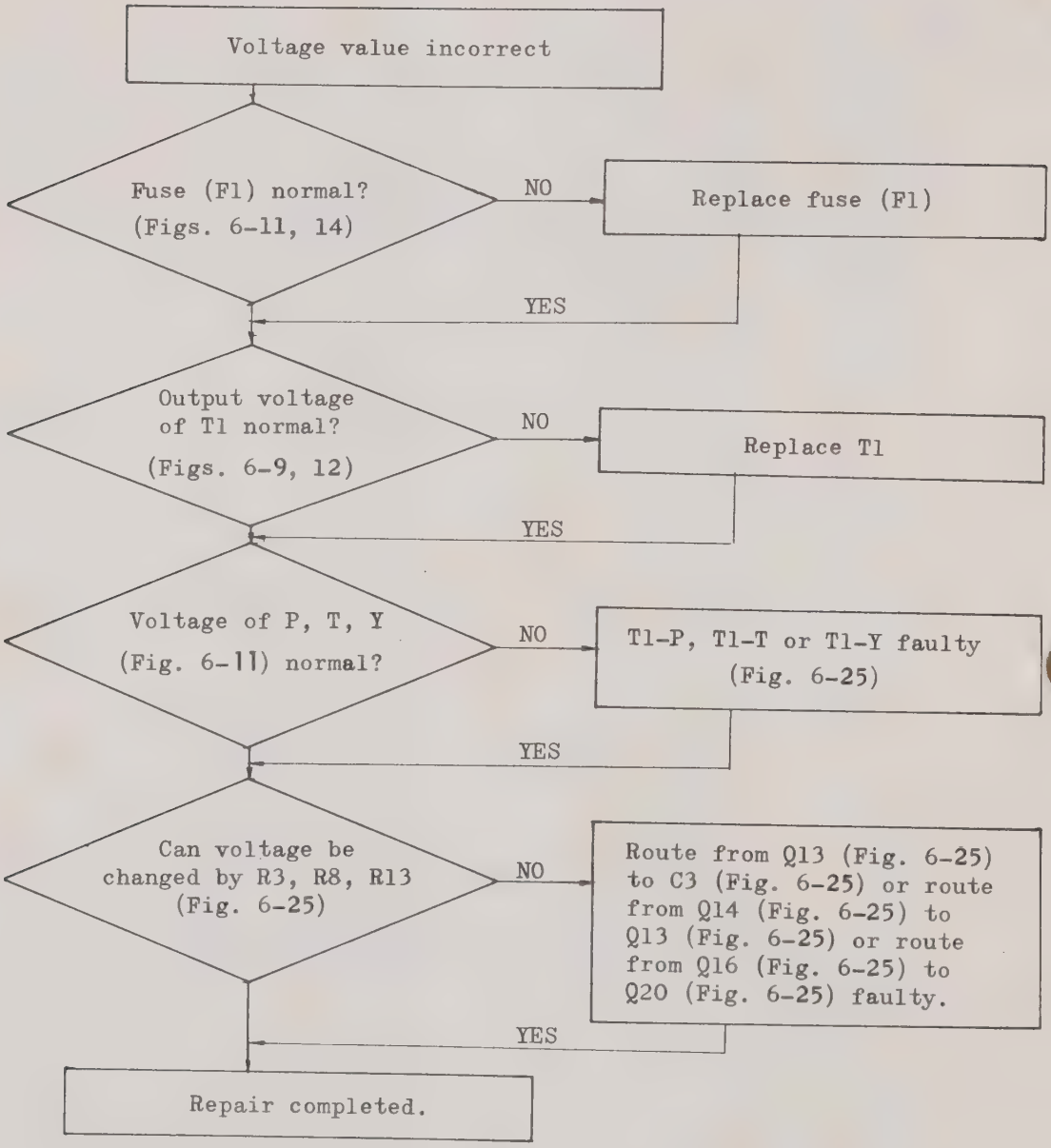


Figure 6-15 Flow Chart for Repair When Voltage Value is not Correct

To check (ii), follow flow chart in Figure 6-16.

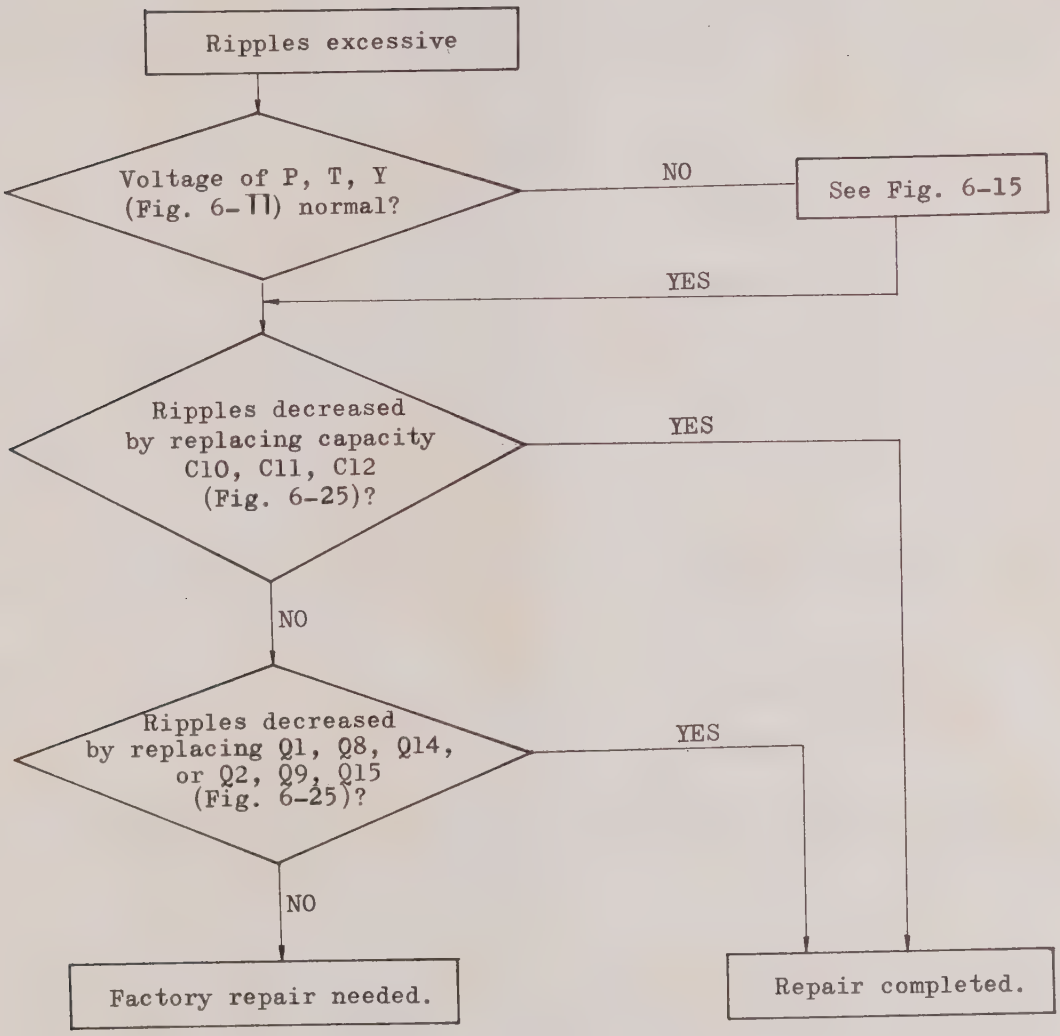


Figure 6-16 Flow Chart for Repair When Ripples are Excessive

Table 6-2 Voltage Values at Major Points-1

Standard values are listed below.

Measuring Point	Voltage	Purpose
P (Fig. 6-11)	+8.3 V	
T (Fig. 6-11)	+8.6 V	
Y (Fig. 6-11)	+20.0 V	
Terminal 2 of R3 (Fig. 6-25)	-10.20 V	Establishes -12 V
Terminal 2 of R8 (Fig. 6-25)	-3.45 V	Establishes -2 V, -5.2 V
Terminal 2 of R10 (Fig. 6-25)	-4.39 V	Establishes -2 V
Terminal 2 of R13 (Fig. 6-25)	+1.78 V	Establishes +5 V, +12 V
Terminal 2 of R15 (Fig. 6-25)	+6.34 V	Establishes +5 V

6.2.2 Clock Signal Output Abnormal

Follow flow chart in Figure 6-17.

Table 6-3 lists the voltage values at major points. Figure 6-31 shows a normal pulse waveform and Figure 6-26, the **printboard.** The route-to-route level is the TTL level.

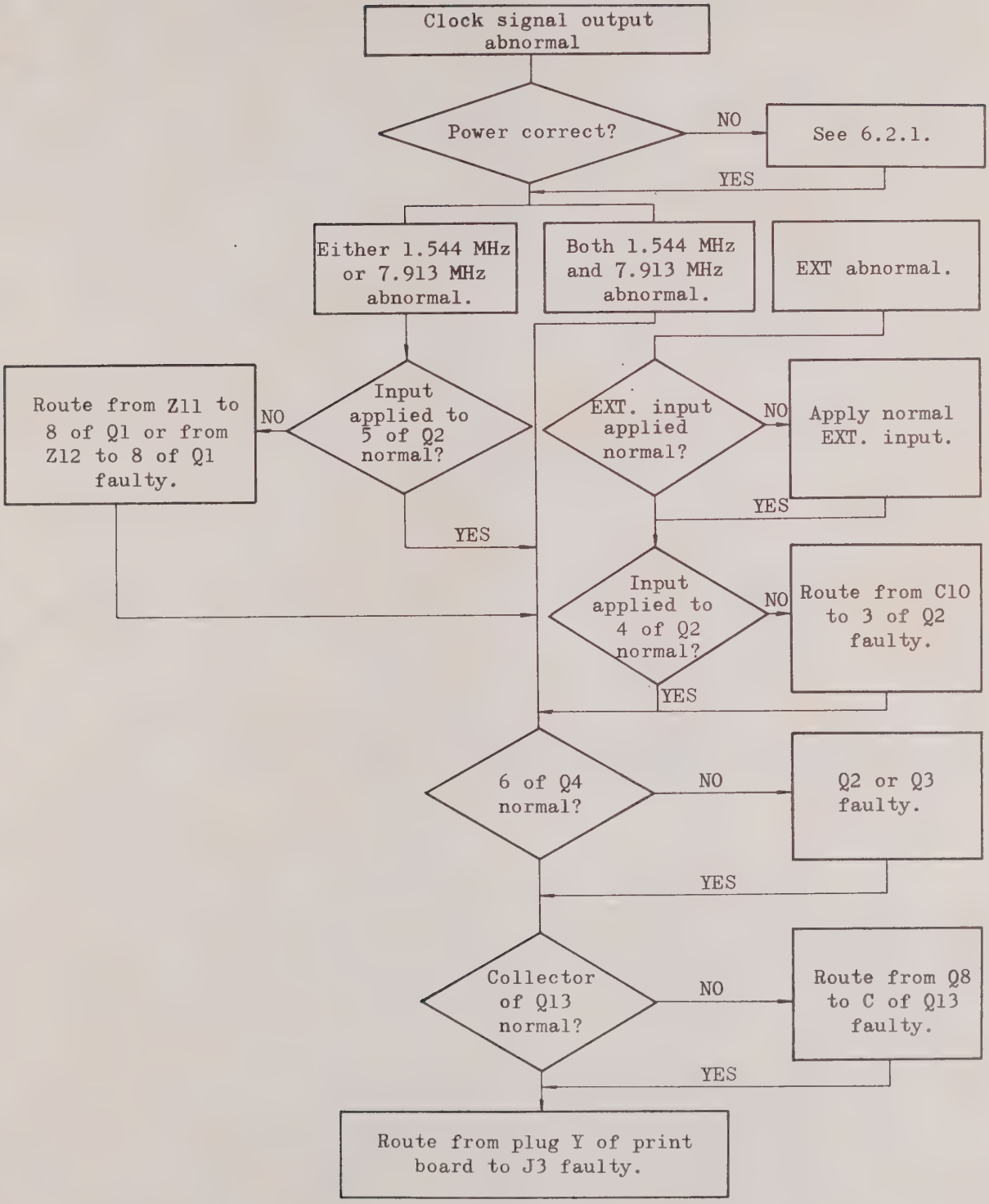


Figure 6-17 Flow Chart for Repair When Clock Signal Output is Abnormal

Table 6-3 Voltage Values at Major Points-2

The standard values are shown below:

Measuring Point	Voltage
Q1 side of C8	+1. 10 V
Q1 side of C9	+1. 11 V
R10 side of C10	-0. 19 V
Between R15 and R16	-0. 24 V
Between R23 and R24	-4. 18 V
Between R32 and R33	+9. 49 V

6. 2. 3 Pattern Signal Output Abnormal

Check as in Figure 6-18.

Table 6-4 lists the voltage values at major points.

Figure 6-31 shows a normal waveform and Figure 6-27 the printboard. The route-to-route level is the TTL level.

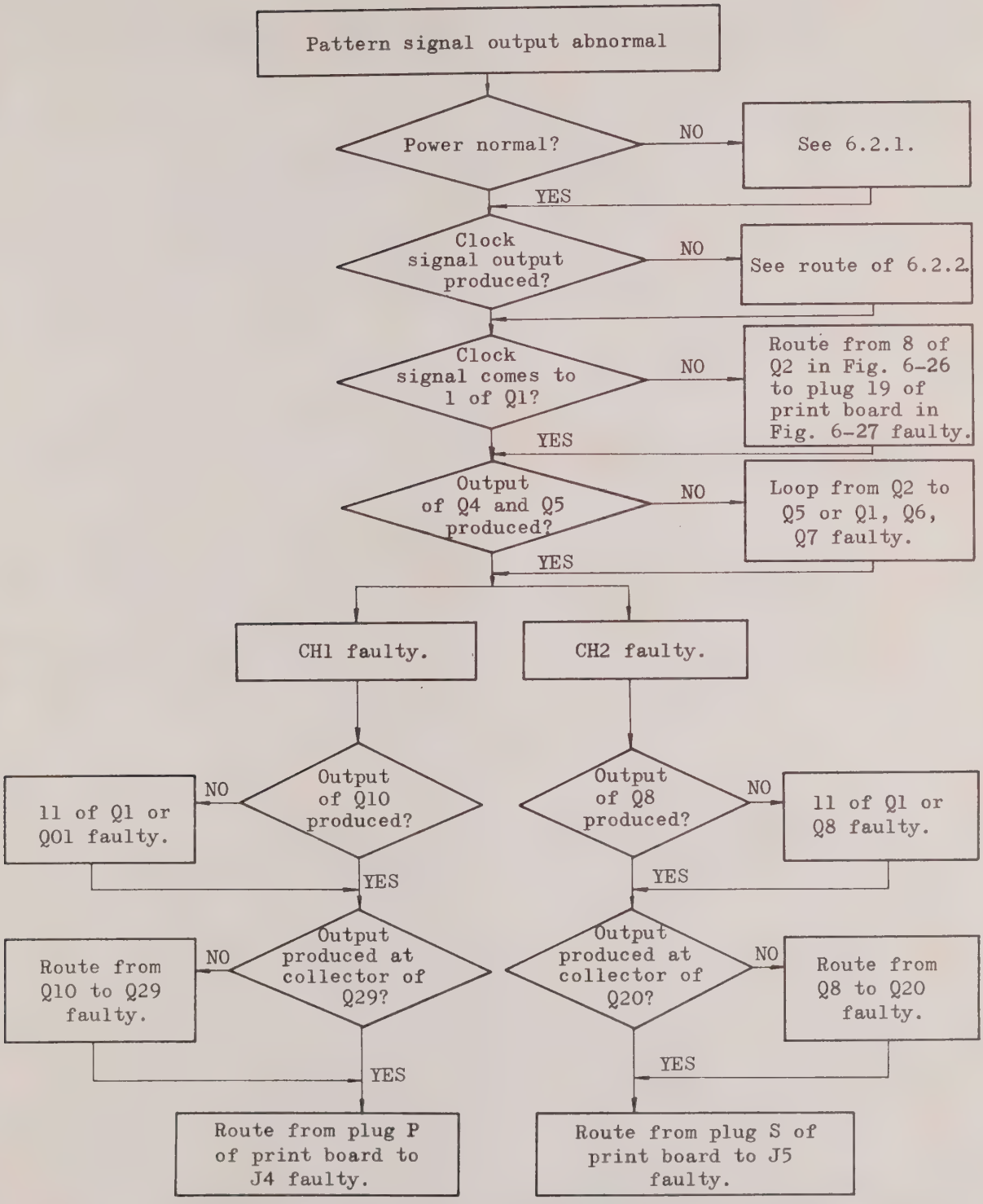


Figure 6-18 Flow Chart for Repair When Pattern Signal Output is Abnormal

Table 6-4 Voltage Values at Major Points-3

Standard values are as follows.

Measuring Point	Voltage
Between R16 and R17	+7.24 V
Between R34 and R35	+7.25 V

6.2.4 INPUT ALARM Lamp Abnormal

Two different phenomena are involved. Thus, check according to Figure 6-19 or Figure 6-20.

The voltage values at major points are listed in Table 6-5.

Figure 6-25 shows the printboard. The route-to-route level is the TTL level.

Phenomenon 1

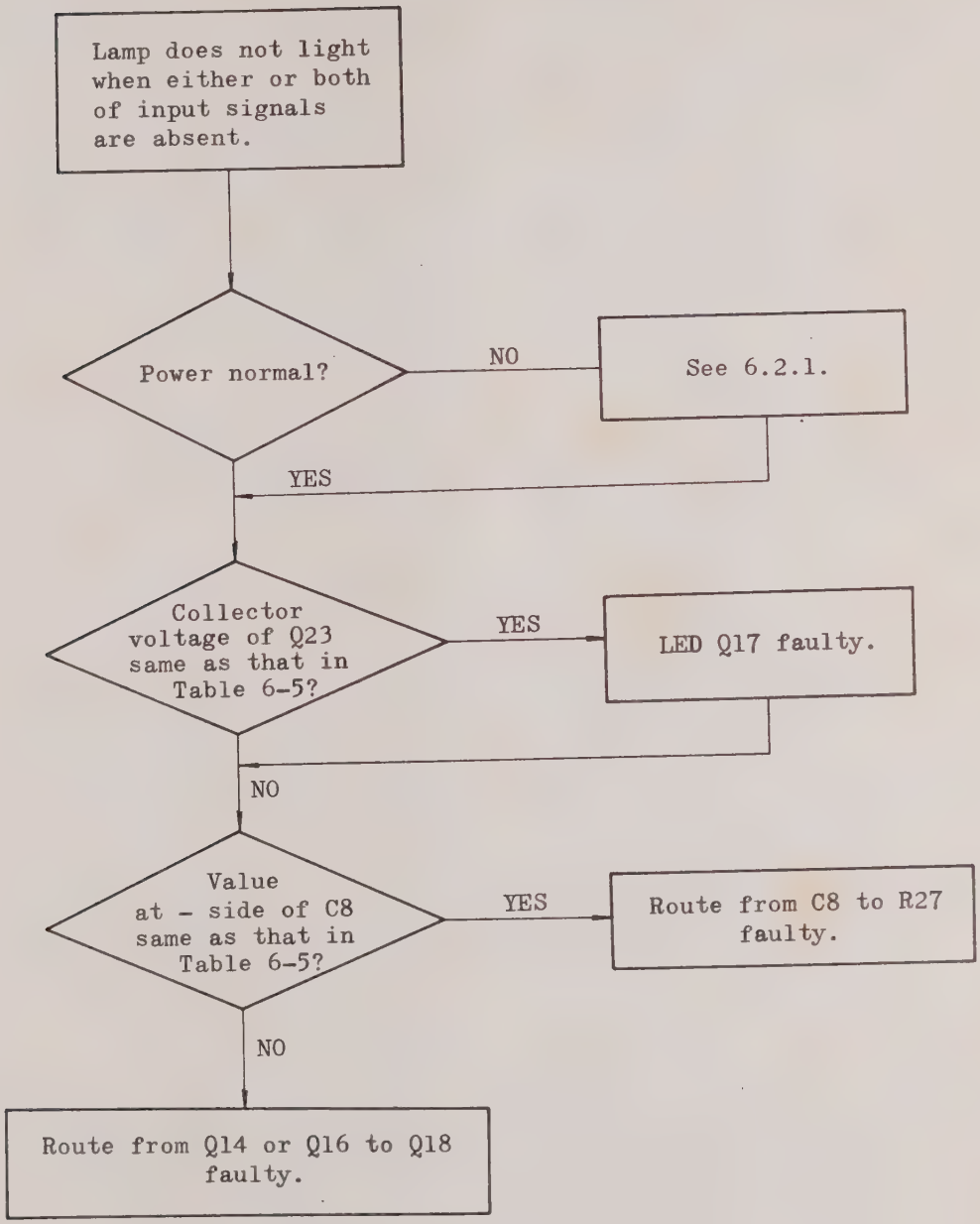

Lamp does not light when either or both of input signals are absent.
Power normal?
NO
See 6.2.1.
YES
Collector voltage of Q23 same as that in Table 6-5?
YES
LED Q17 faulty.
NO
Value at - side of C8 same as that in Table 6-5?
YES
Route from C8 to R27 faulty.
NO
Route from Q14 or Q16 to Q18 faulty.

Figure 6-19 Flow Chart for Repair When Lamp does not Light as Required

Phenomenon 2

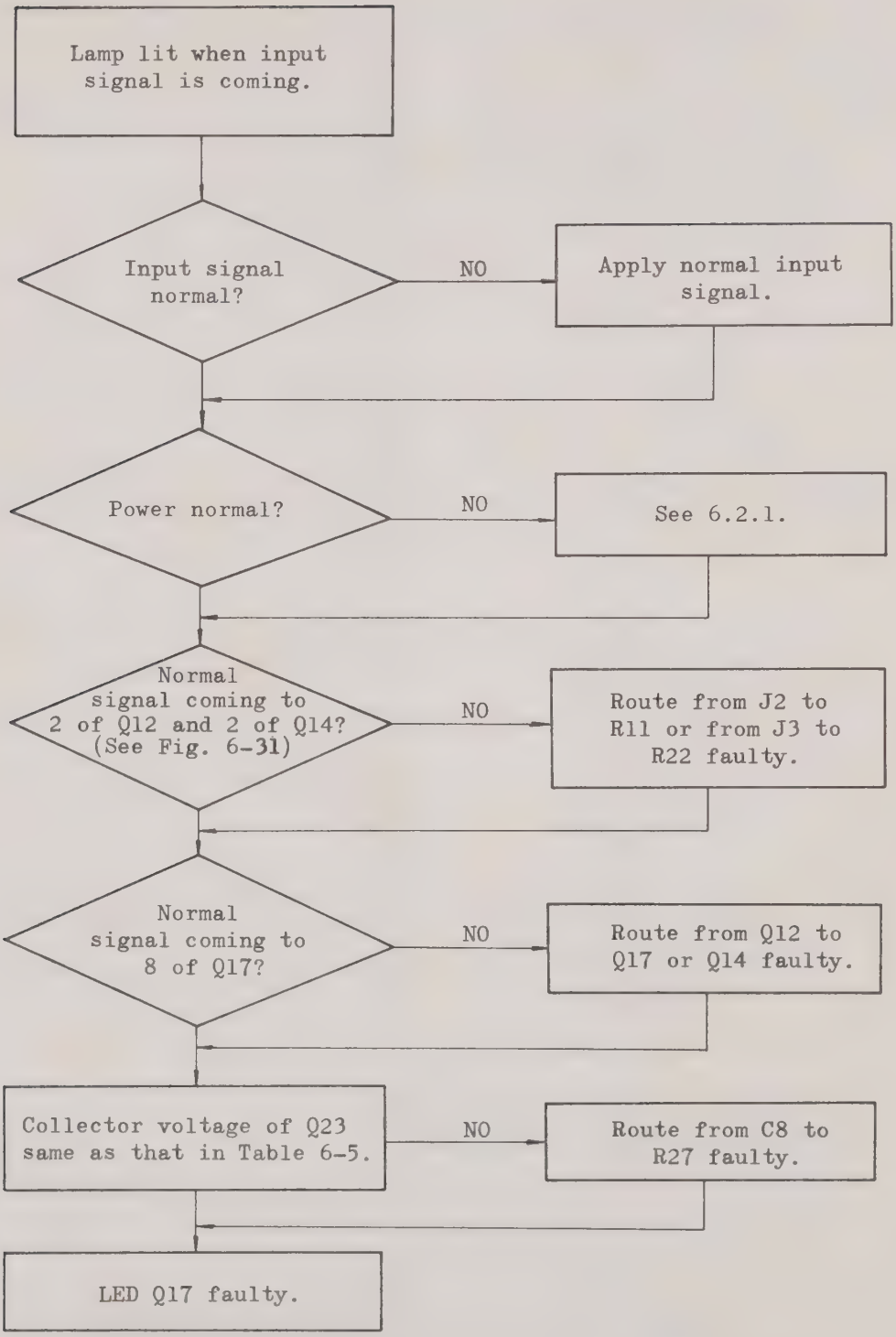

Lamp lit when input signal is coming.
Input signal normal?
NO
Apply normal input signal.
Power normal?
NO
See 6.2.1.
Normal signal coming to 2 of Q12 and 2 of Q14? (See Fig. 6-31)
NO
Route from J2 to R11 or from J3 to R22 faulty.
Normal signal coming to 8 of Q17?
NO
Route from Q12 to Q17 or Q14 faulty.
Collector voltage of Q23 same as that in Table 6-5.
NO
Route from C8 to R27 faulty.
LED Q17 faulty.

Figure 6-20 Flow Chart for Repair When Lamp although not Lights Required

Table 6-5 Voltage Values at Major Points-4

The standard values are as follows.

Measuring Points	Voltage
Between R9 and R10	-0.46 V
Between R20 and R21	-0.28 V
- side of C8	-0.33 V
Terminal 2 of R27	-1.59 V
Q23 Collector (When LED is on)	-1.66 V
Q23 Collector (When LED is off)	-1.27 V

6.2.5 ERROR Lamp Abnormal

Check as in Figure 6-21. Two phenomena are considered; one with the lamp lit when there is no error and the other, with the lamp not lit when error is present. The same check methods can be applied to both phenomena. Figs. 6-28 and 6-29 show the printboards. The route-to-route level is the TTL level.

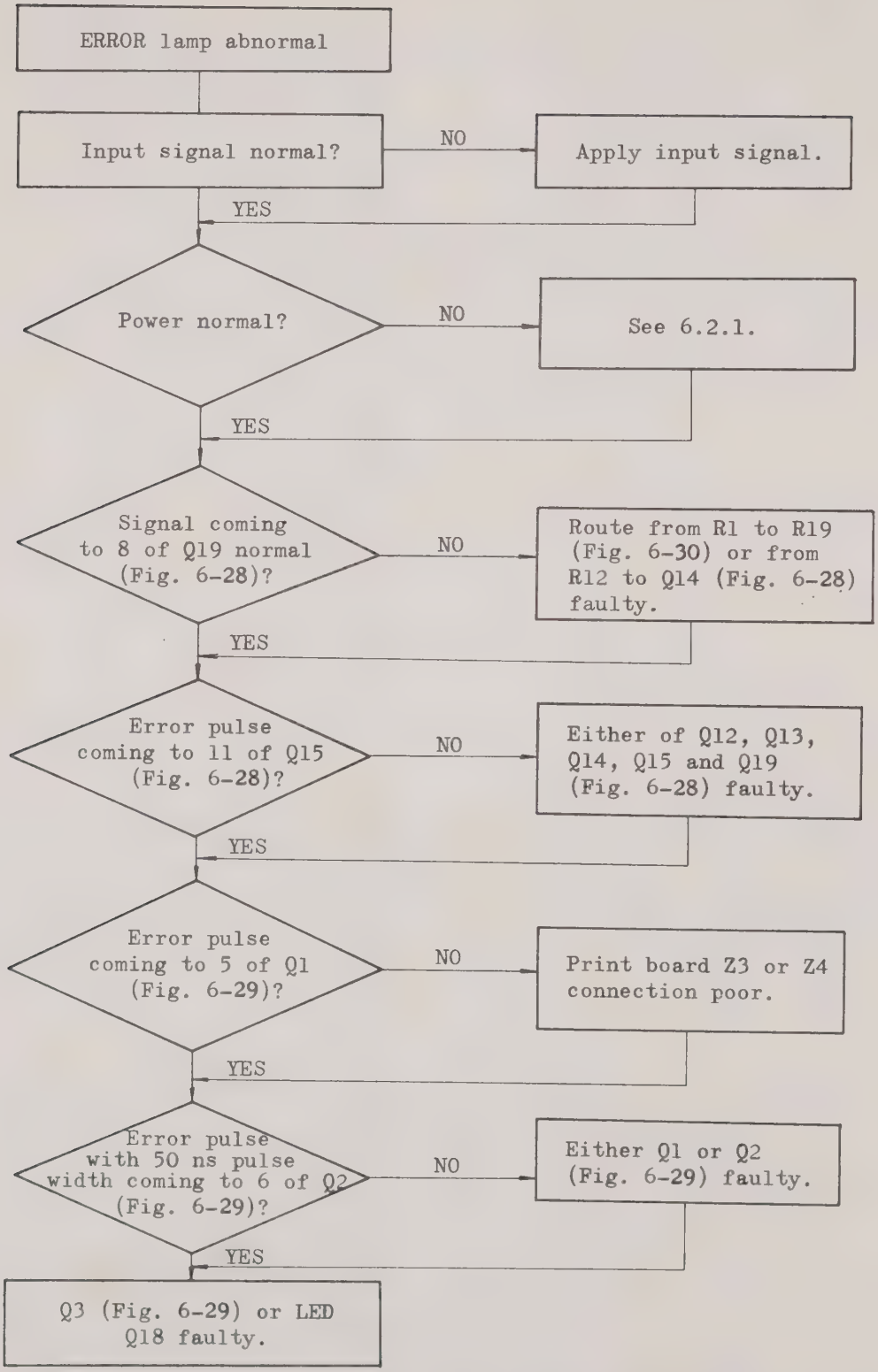

ERROR lamp abnormal
Input signal normal?
NO
Apply input signal.
YES
Power normal?
NO
See 6.2.1.
YES
Signal coming to 8 of Q19 normal (Fig. 6-28)?
NO
Route from R1 to R19 (Fig. 6-30) or from R12 to Q14 (Fig. 6-28) faulty.
YES
Error pulse coming to 11 of Q15 (Fig. 6-28)?
NO
Either of Q12, Q13, Q14, Q15 and Q19 (Fig. 6-28) faulty.
YES
Error pulse coming to 5 of Q1 (Fig. 6-29)?
NO
Print board Z3 or Z4 connection poor.
YES
Error pulse with 50 ns pulse width coming to 6 of Q2 (Fig. 6-29)?
NO
Either Q1 or Q2 (Fig. 6-29) faulty.
YES
Q3 (Fig. 6-29) or LED Q18 faulty.

Figure 6-21 Flow Chart for Repair When ERROR Lamp is Abnormal

6.2.6 Error Output Abnormal

Check as in Figure 6-22.

Figure 6-29 shows the printboard. The route-to-route level is the TTL level.

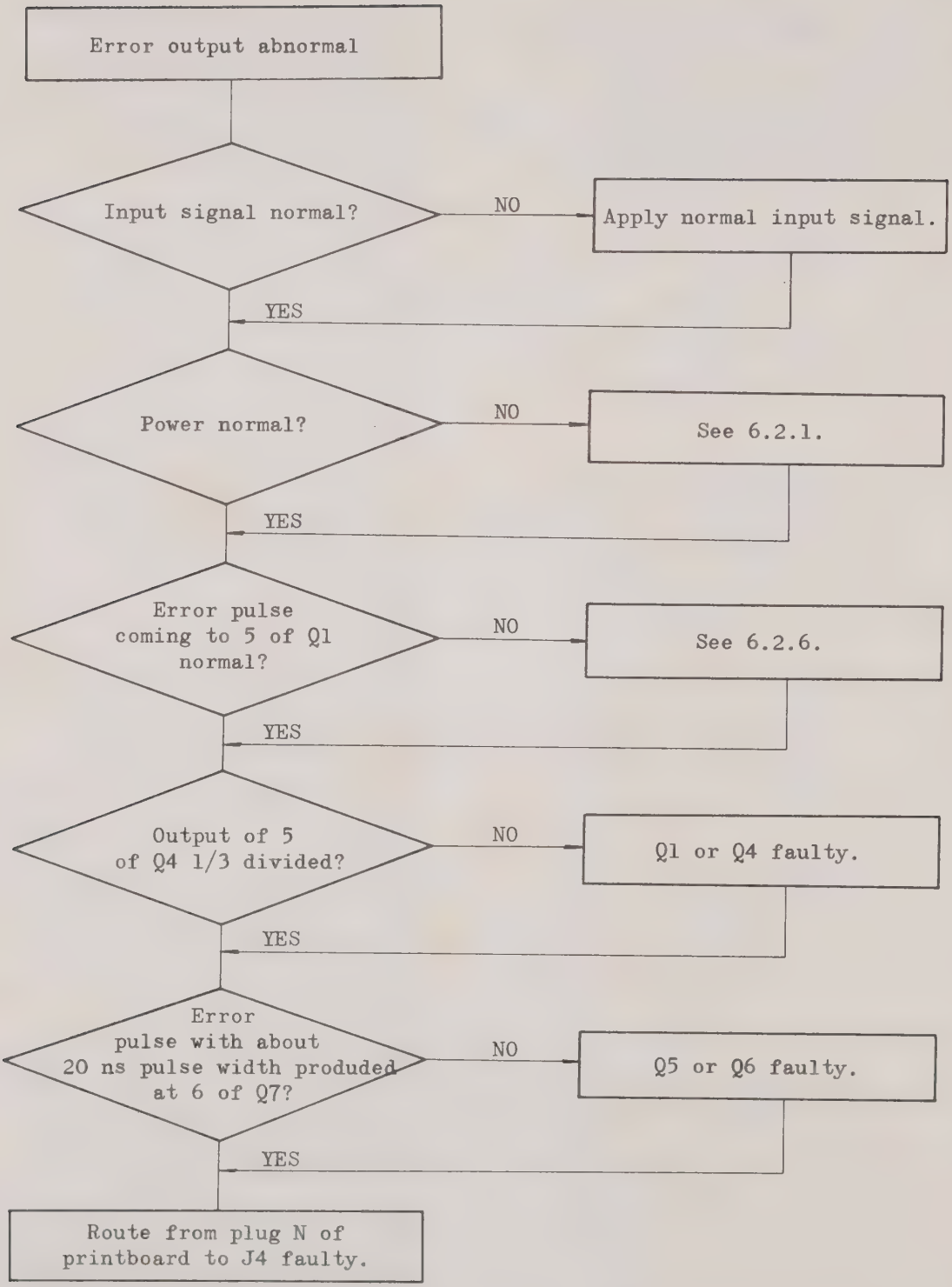


Figure 6-22 Flow Chart for Repair When Error Output is Normal

6.2.7 Meter Indication Abnormal

Check as in Figure 6-23.

Figures 6-29 and 6-30 show the printboard. The route-to-route level is the TTL level.

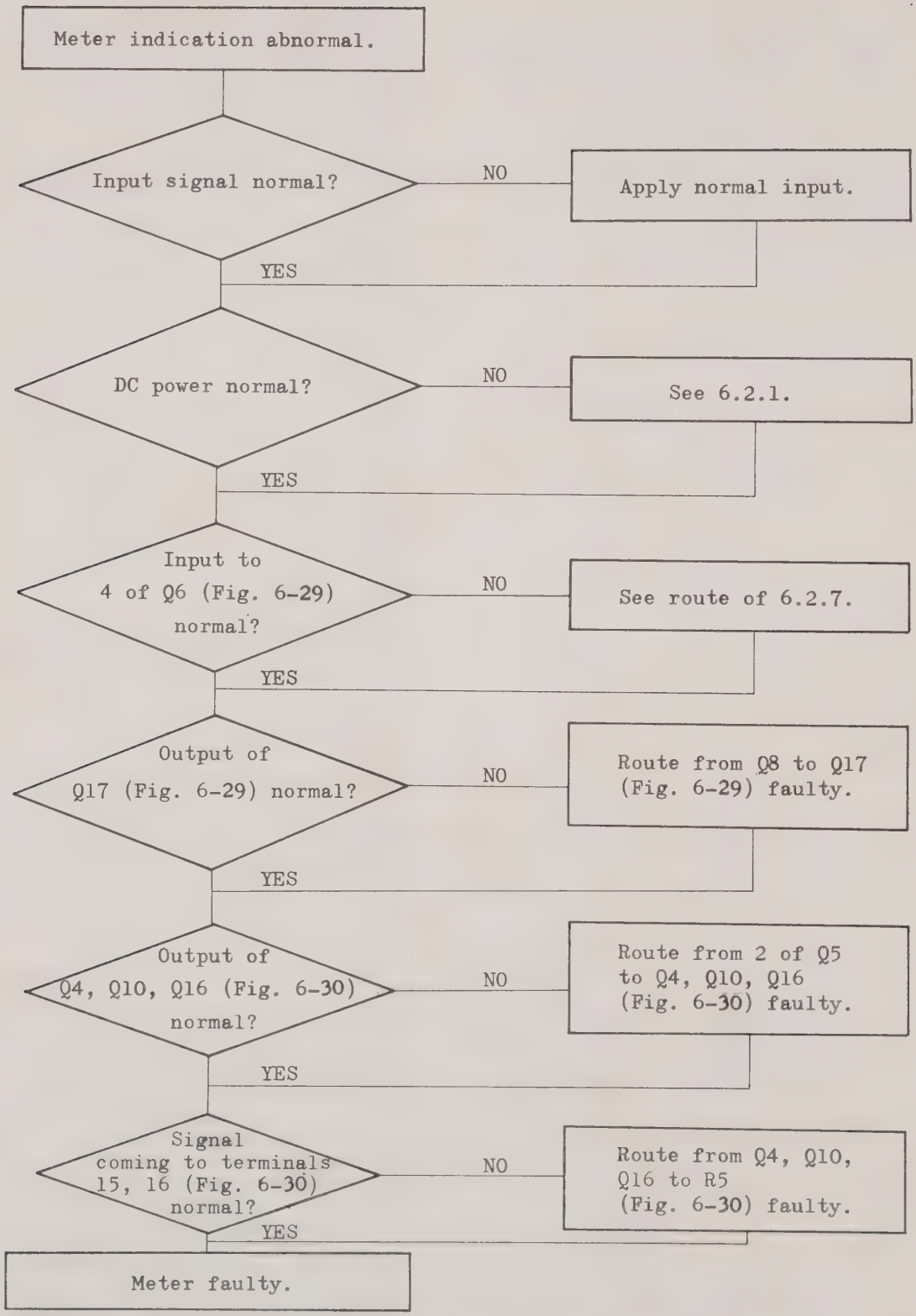


Figure 6-23 Flow Chart for Repair When Meter Indication is Abnormal

6.2.8 OVER FLOW Lamp Abnormal

Check as in Figure 6-24. Figure 6-30 shows the printboard. The route-to-route level is the TTL level.

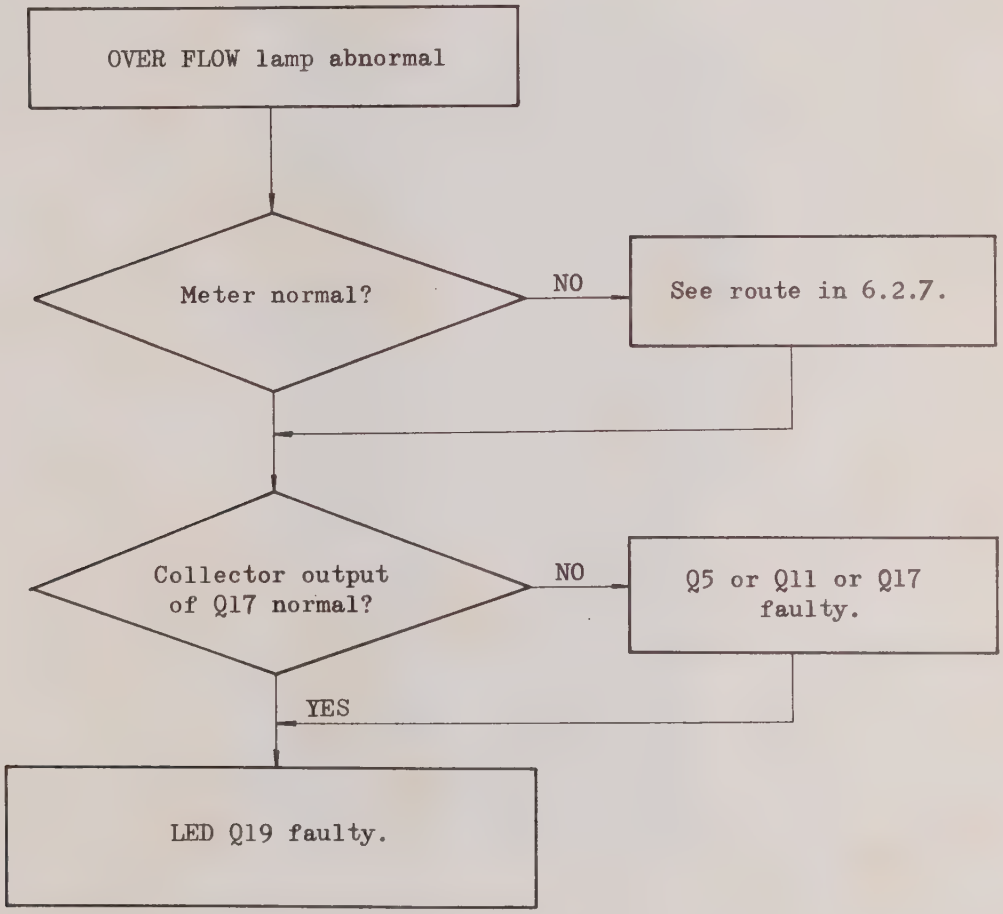


Figure 6-24 Flow Chart for Repair When OVER FLOW Lamp is Abnormal

6.2.9 Component Layout

The layout of components in the printboard are as illustrated below.

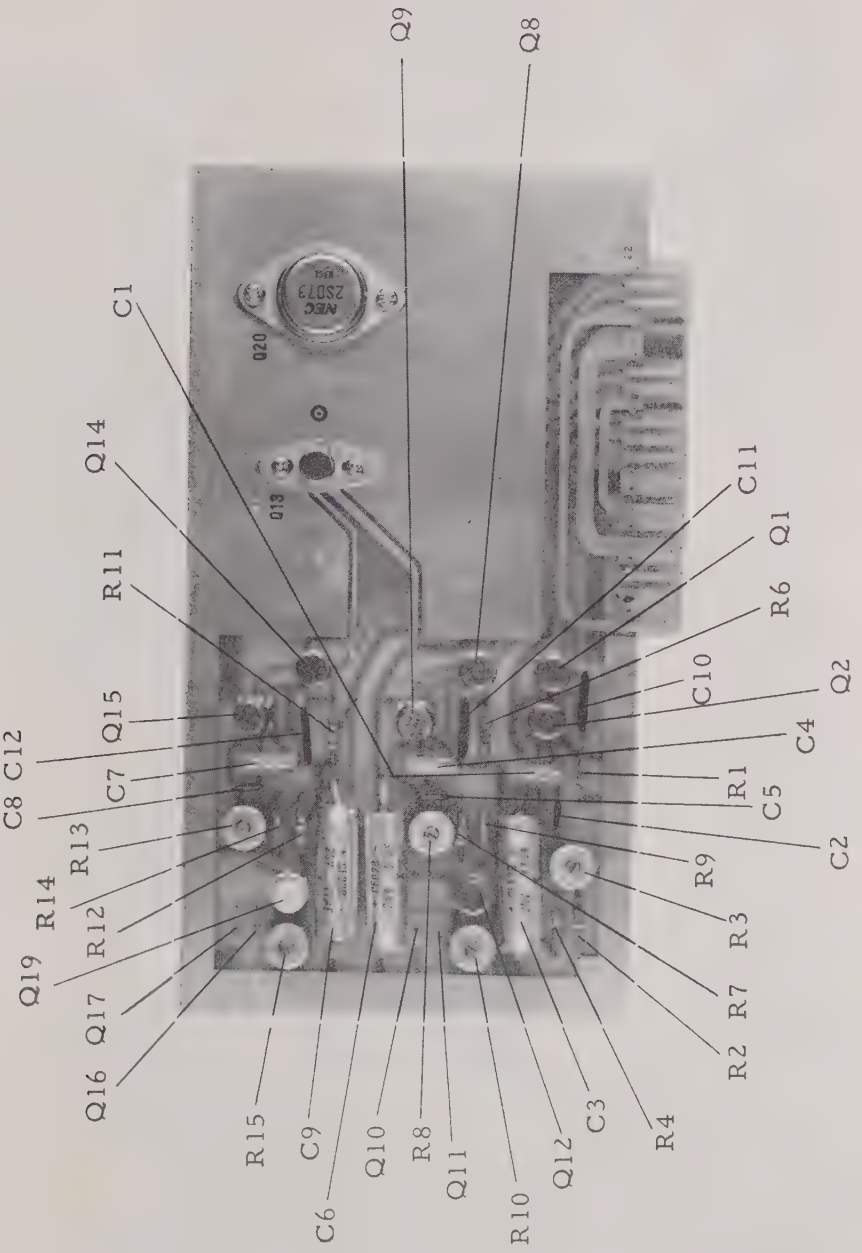


Figure 6-25 432U13235 Voltage Stabilizer

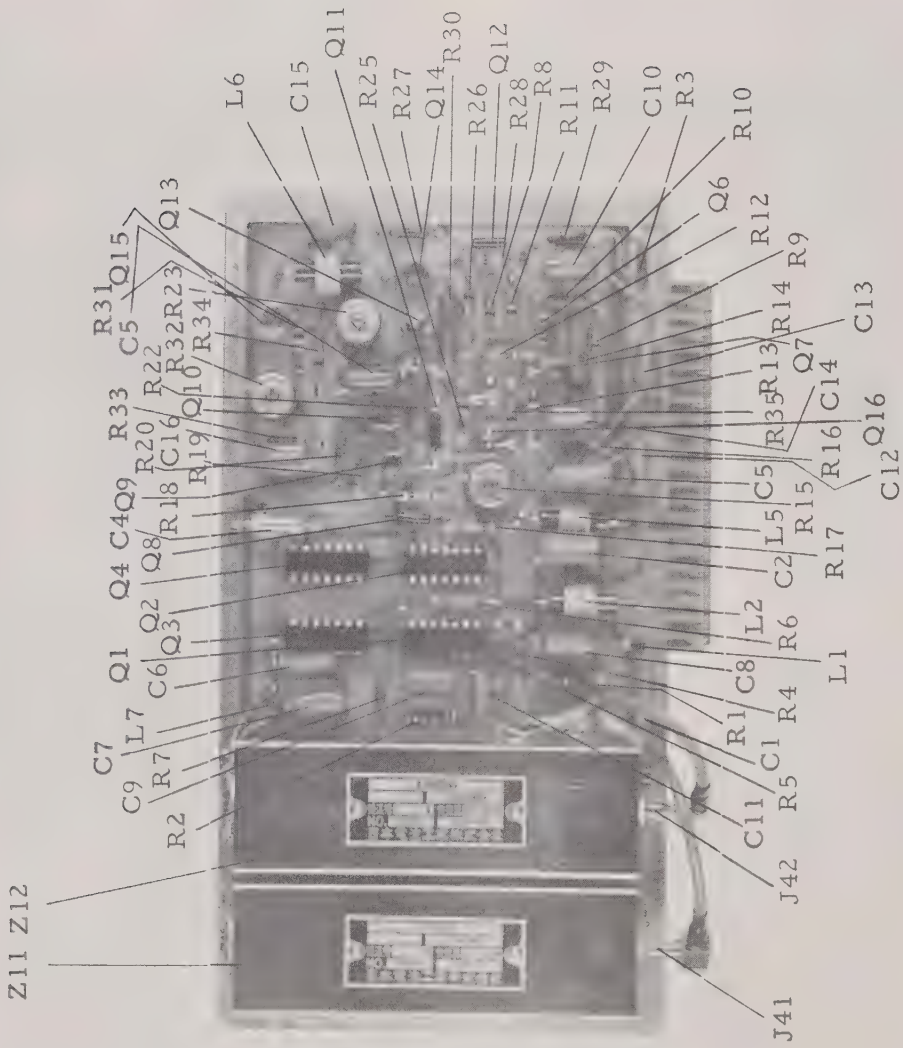


Figure 6-26 432U13634 Clock Circuit

Figure 6-27 432U13635 Pattern Generator

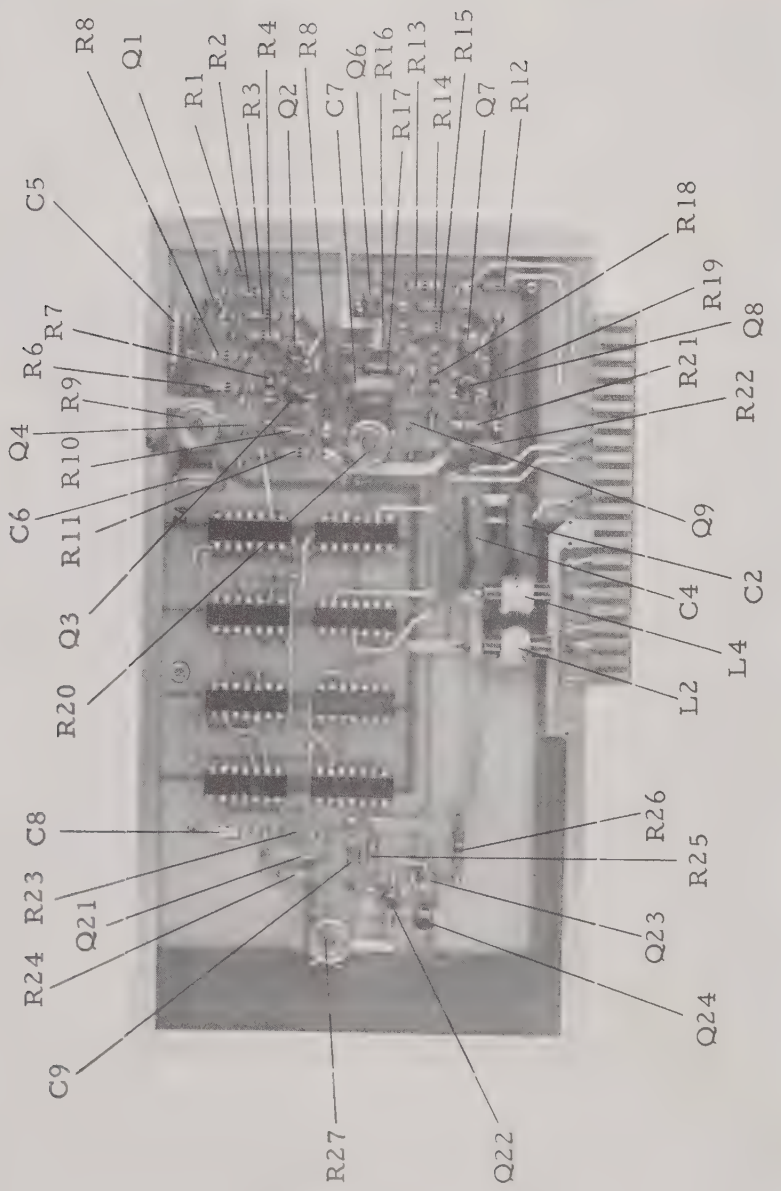


Figure 6-28 432U13636 Error Detecting Circuit

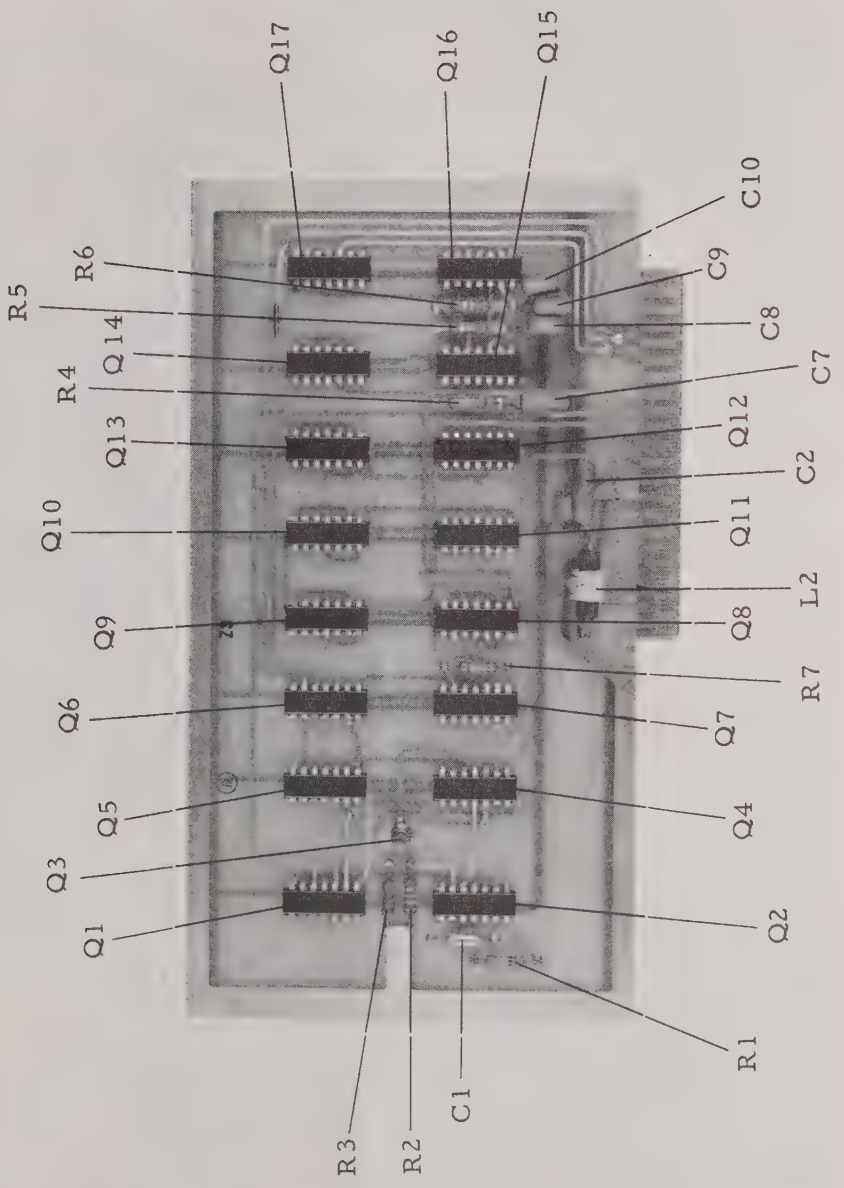


Figure 6-29 432U13637 Time Base Circuit

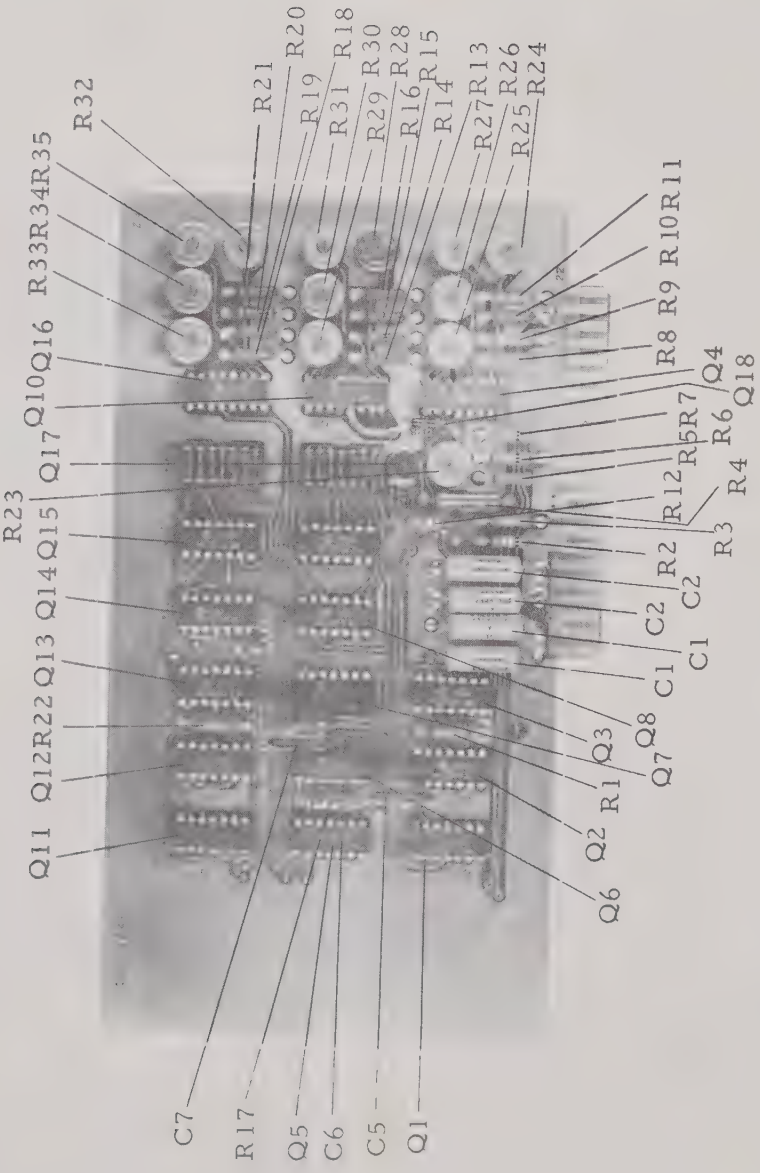
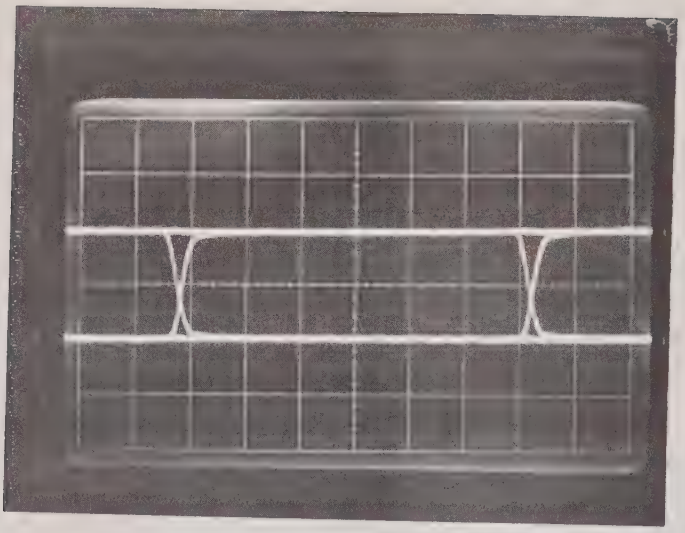


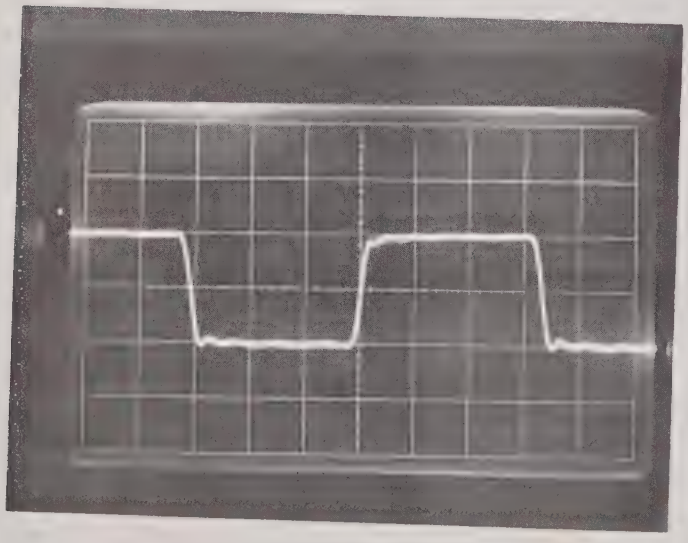
Figure 6-30 432U13848 Meter Indication Circuit

6.2.10 Waveforms Illustrated



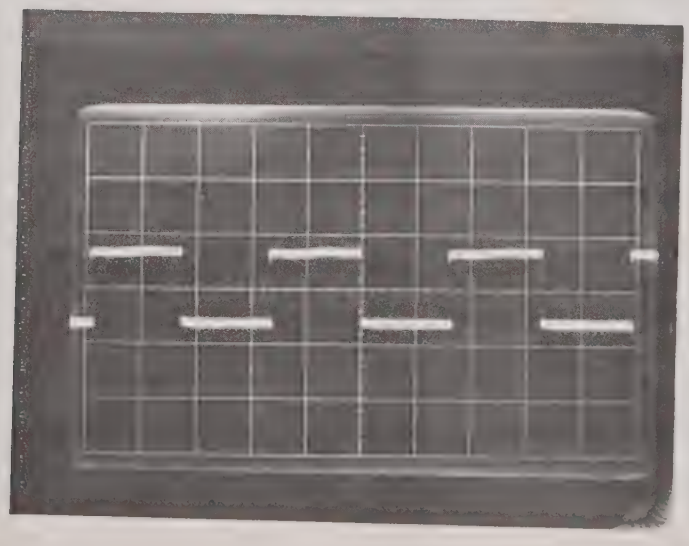
Pattern Signal

DATA:
1 V/diV
20 ns/diV



Clock Signal

DATA:
1 V/diV
20 ns/diV



Synchronizing Output

DATA:
1 V/diV
5 μs/diV

Figure 6-31 Waveforms

6.3 STORAGE

The ME422A Error Rate Measuring Equipment should be stored under temperature range of -10°C to +55°C and humidity of 30% to 95%.

If equipment previously stored in a room with low temperature (in the vicinity of 0°C) is brought into a room with normal temperature, it would catch moisture which can cause short circuit or damage the insulation. In such a case, it would be better to leave the equipment in the room with normal temperature for approximately 3 hours before power is first applied.

SECTION VII

DRAWINGS

GENERAL

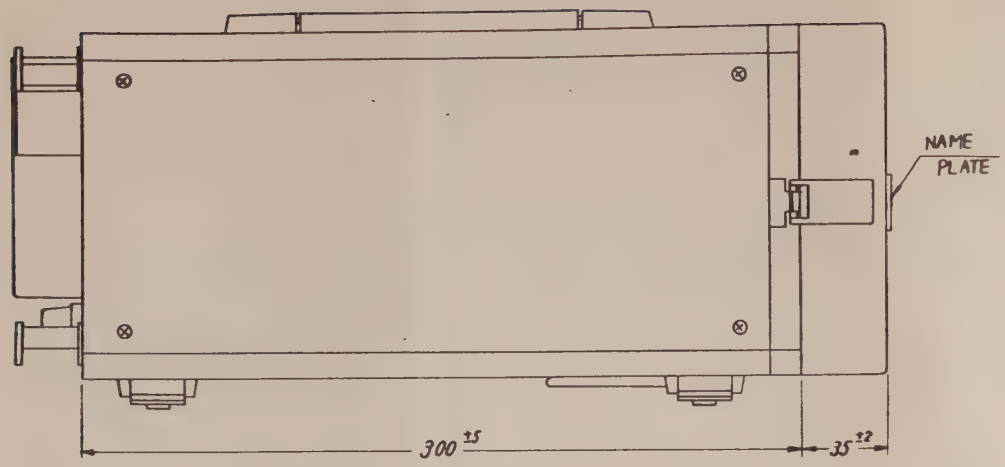
In the circuit diagram, the following units are used for capacity of the condenser and resistance value of the resistor.

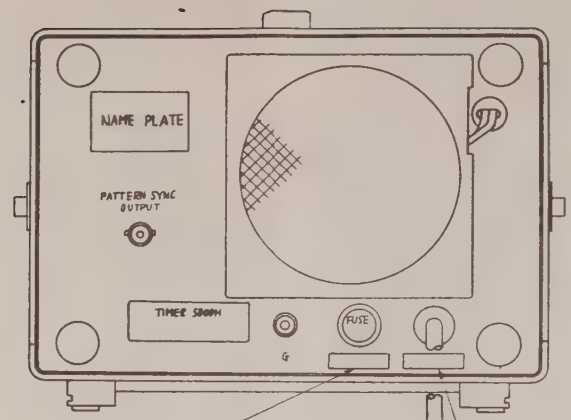
For capacity of condenser

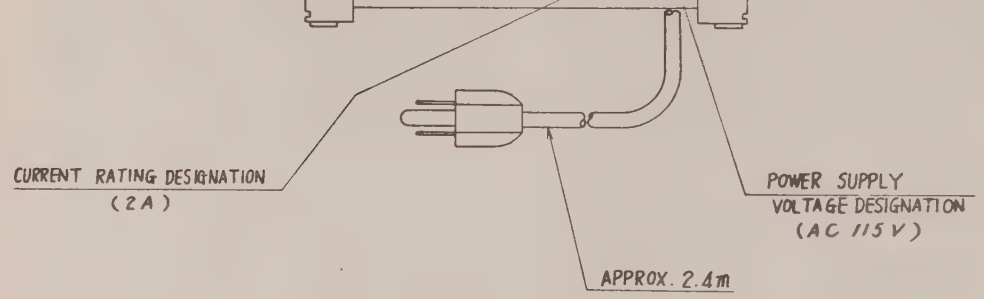
No unit reference	→ μF	Example:	10 → 10 μF
"p"	→ pF	"	5p → 5 pF

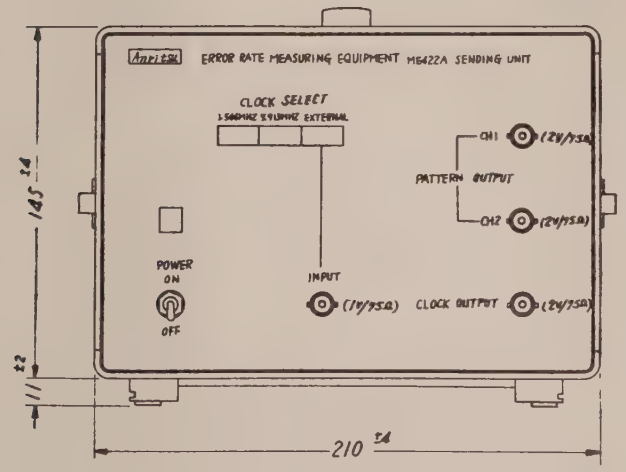
For resistance value of resistor

No unit reference	→	Example:	10 → 10 Ω
"K"	→ kΩ	"	5K → 5 kΩ
"M"	→ MΩ	"	3M → 3 MΩ

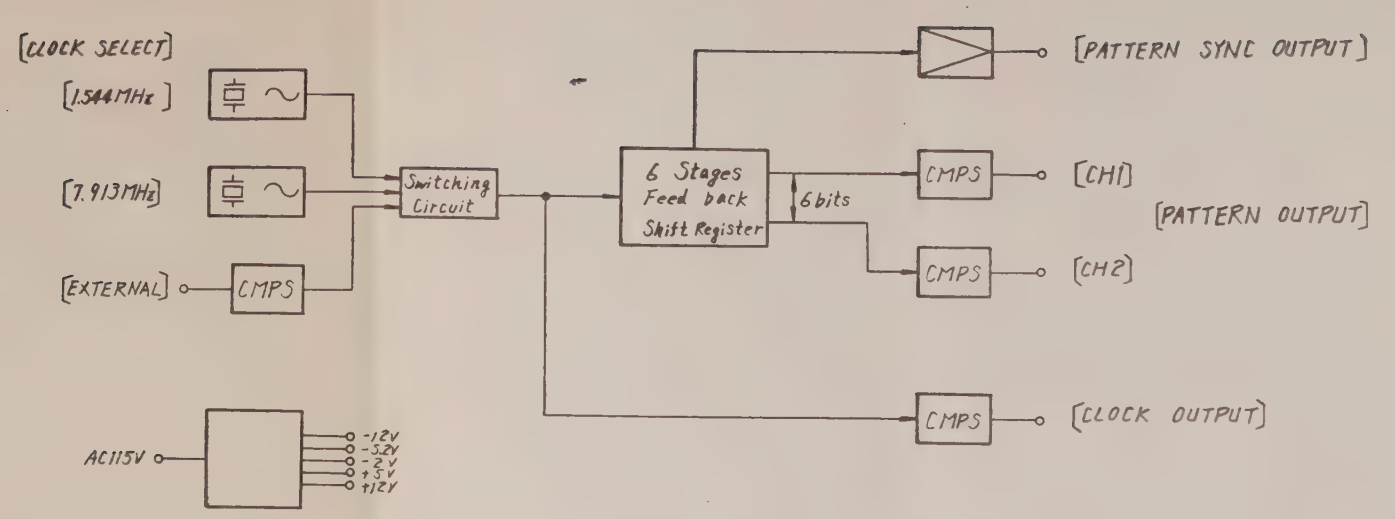








TITLE: FRONT VIEW AND OTHER VIEWS OF ERROR RATE MEASURING EQUIPMENT ME422A SENDING UNIT		
SIZE: C	CODE IDENT NO.: 12859	DRAWING NO.: 49W 1888
SCALE	WEIGHT	SHEET

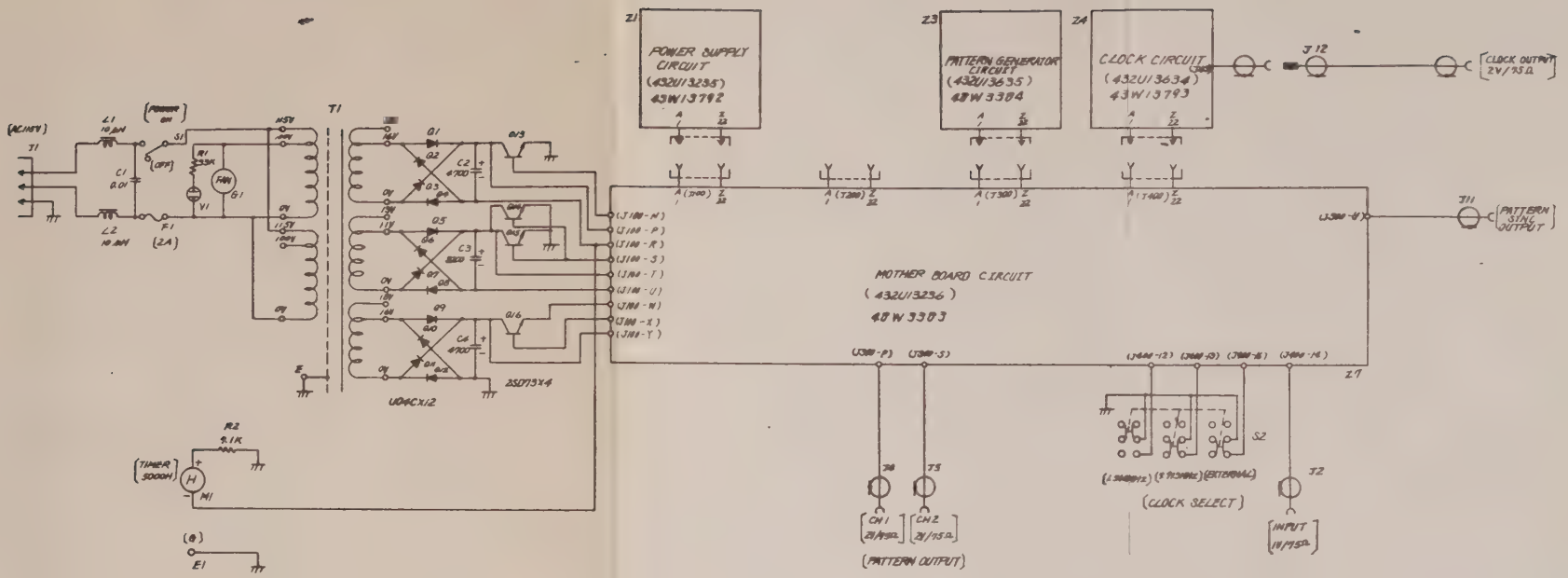


Oscillator

CMPS Current Mode Pulse Shaper

Amplifier

TITLE		
BLOCK DIAGRAM OF ME422A SENDING UNIT		
SIZE B	CODE IDENT NO. 12859	DRAWING NO. 43W13904
SCALE	WEIGHT	SHEET



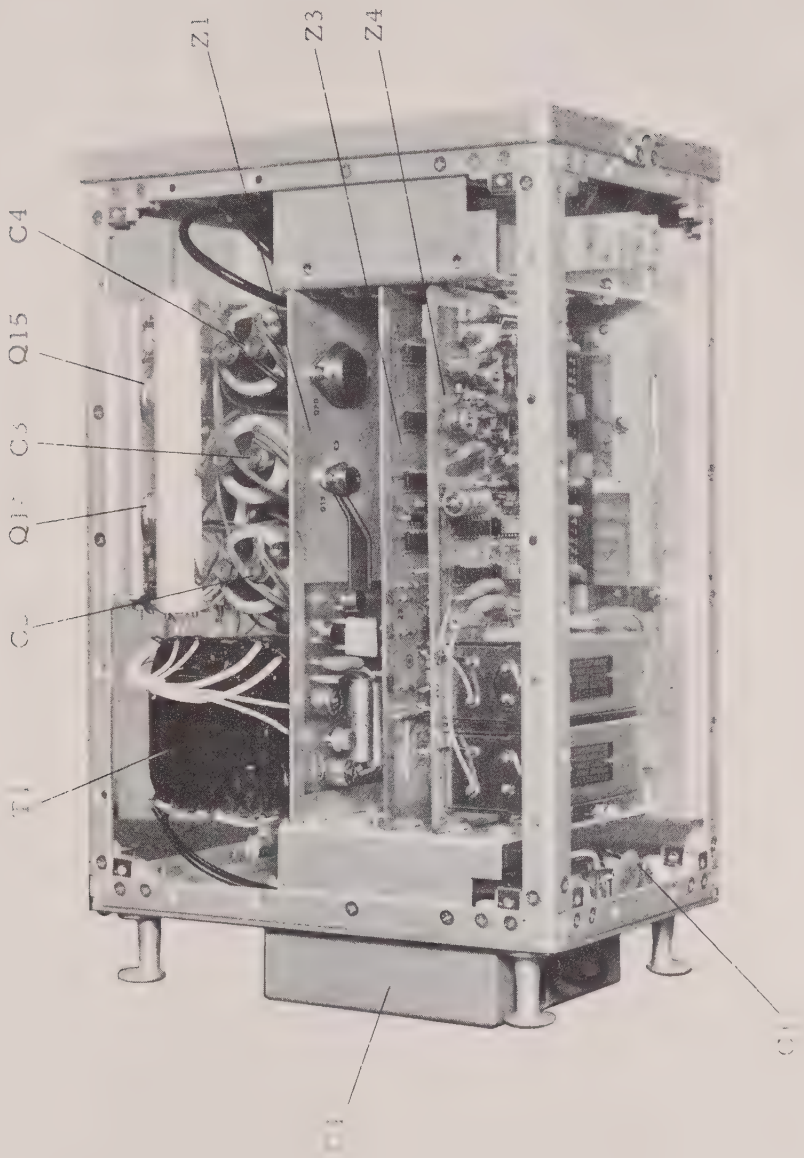
PARTS VALUES LIST

44W42255

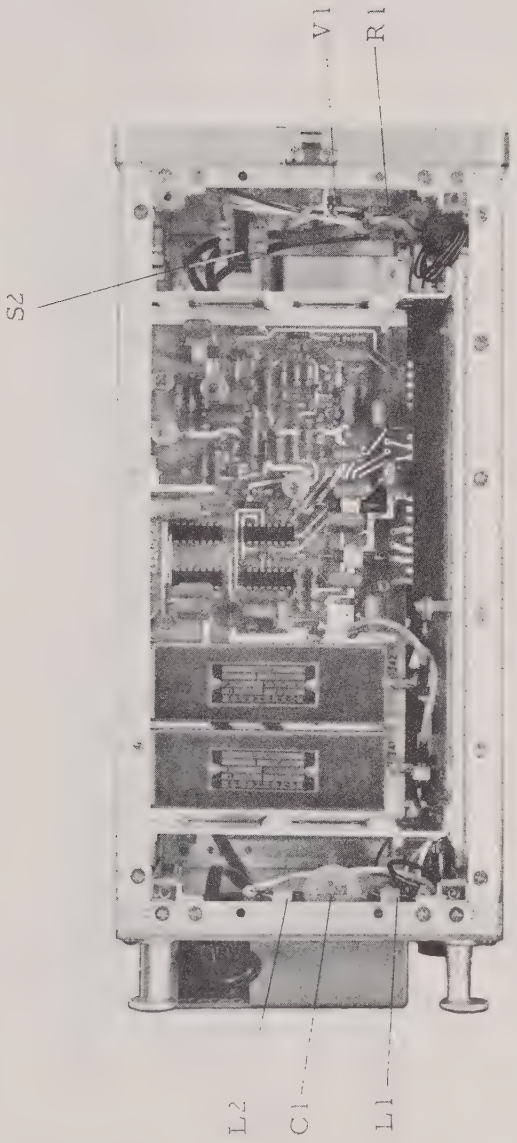
REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	10000pF +80 -20%, 50V		
C2	4700μF +50 -10%, 35V		
C3	8200μF +50 -10%, 25V		
C4	8200μF +50 -10%, 35V		
L1	10μH		
L2	10μH		
R1	33kΩ ±5%, 1/4W		
R2	9.1kΩ ±5%, 1/4W		

TITLE		
CIRCUIT DIAGRAM OF ERROR RATE MEASURING EQUIPMENT ME422A SENDING UNIT		
SIZE: C	CODE IDENT NO: 12859	DRAWING NO: 48W 3382
SCALE	WEIGHT	SHEET

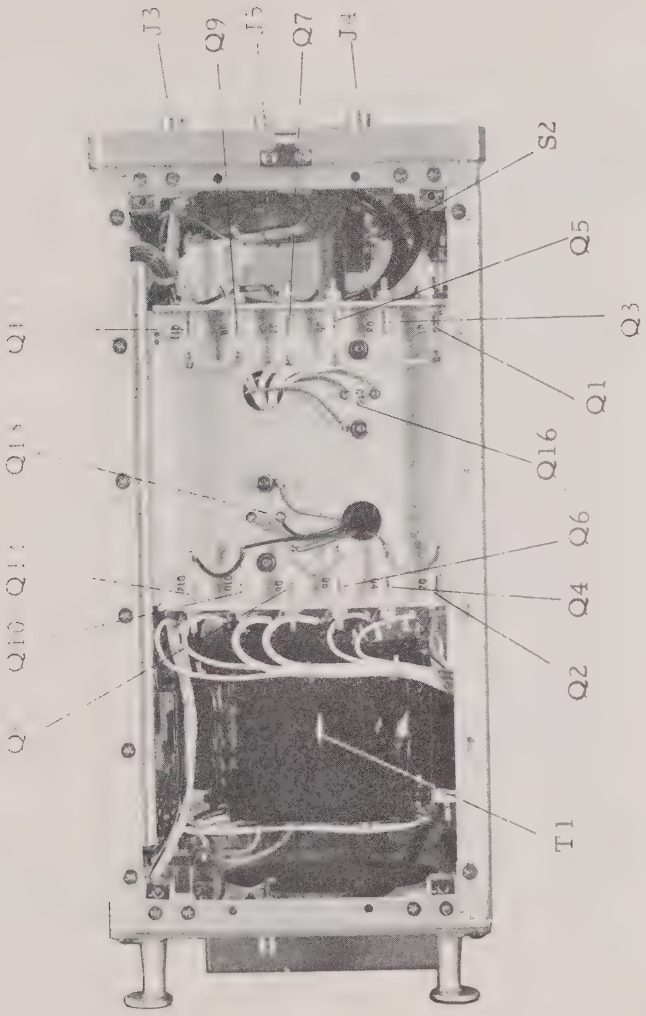
PARTS LIST TO BE SUPPLIED IN FINAL MANUAL



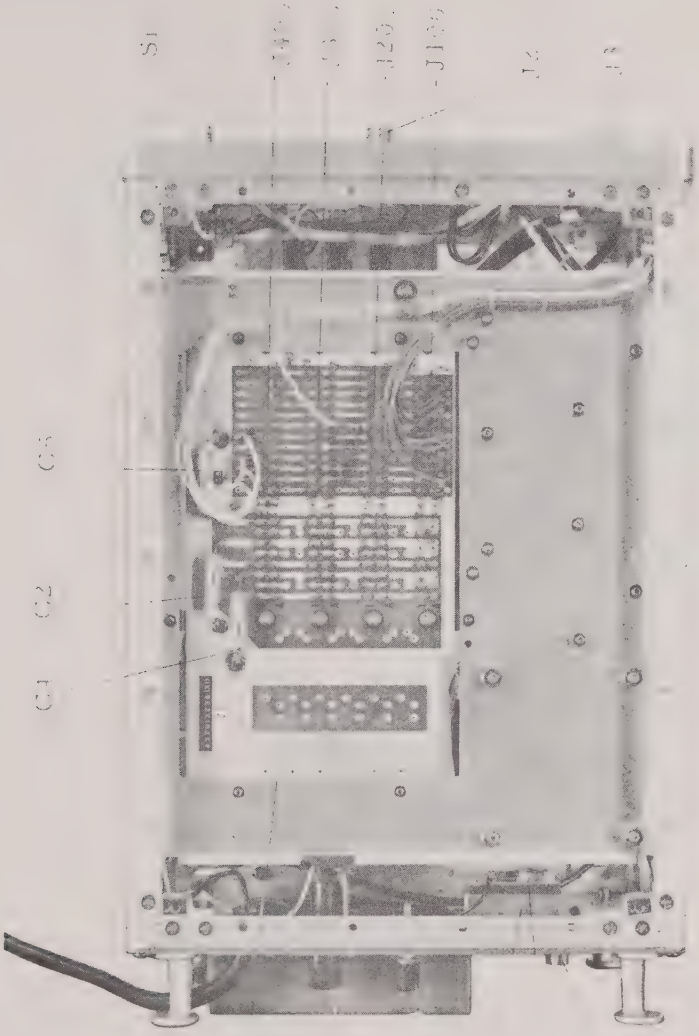
TITLE		
ME422A (SENDING UNIT)		
SIZE A	CODE IDENT NO. 12859	DRAWING NO 4-0
SCALE	WEIGHT	SHEET



TITLE		
	ME422A (SENSING UNIT)	
SIZE A	CODE IDENT NO. 12859	DRAWING NO
SCALE	WEIGHT	SHEET



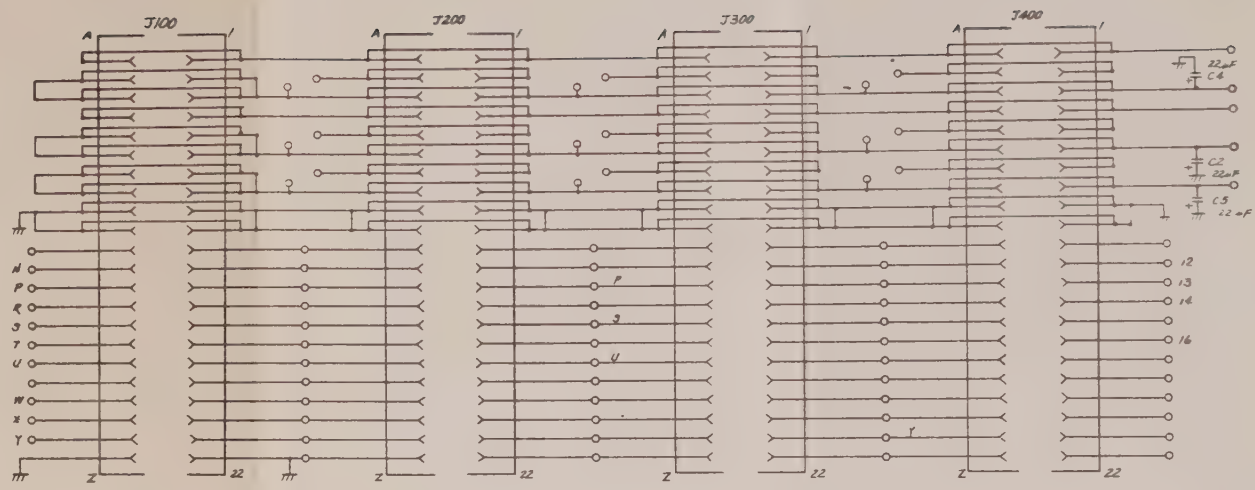
TITLE		
SIZE A	CODE IDENT NO 12859	DRAWING NO
SCALE	WEIGHT	SHEET



TITLE		
SIZE A	CODE IDENT NO. 12859	DRAWING NO
SCALE	WEIGHT	SHEET

PARTS VALUES LIST 44W42256

REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	Not assigned		
C2	22μF +100 -10%, 16V		
C3	Not assigned		
C4 to C5	22μF +100 -10%, 16V		



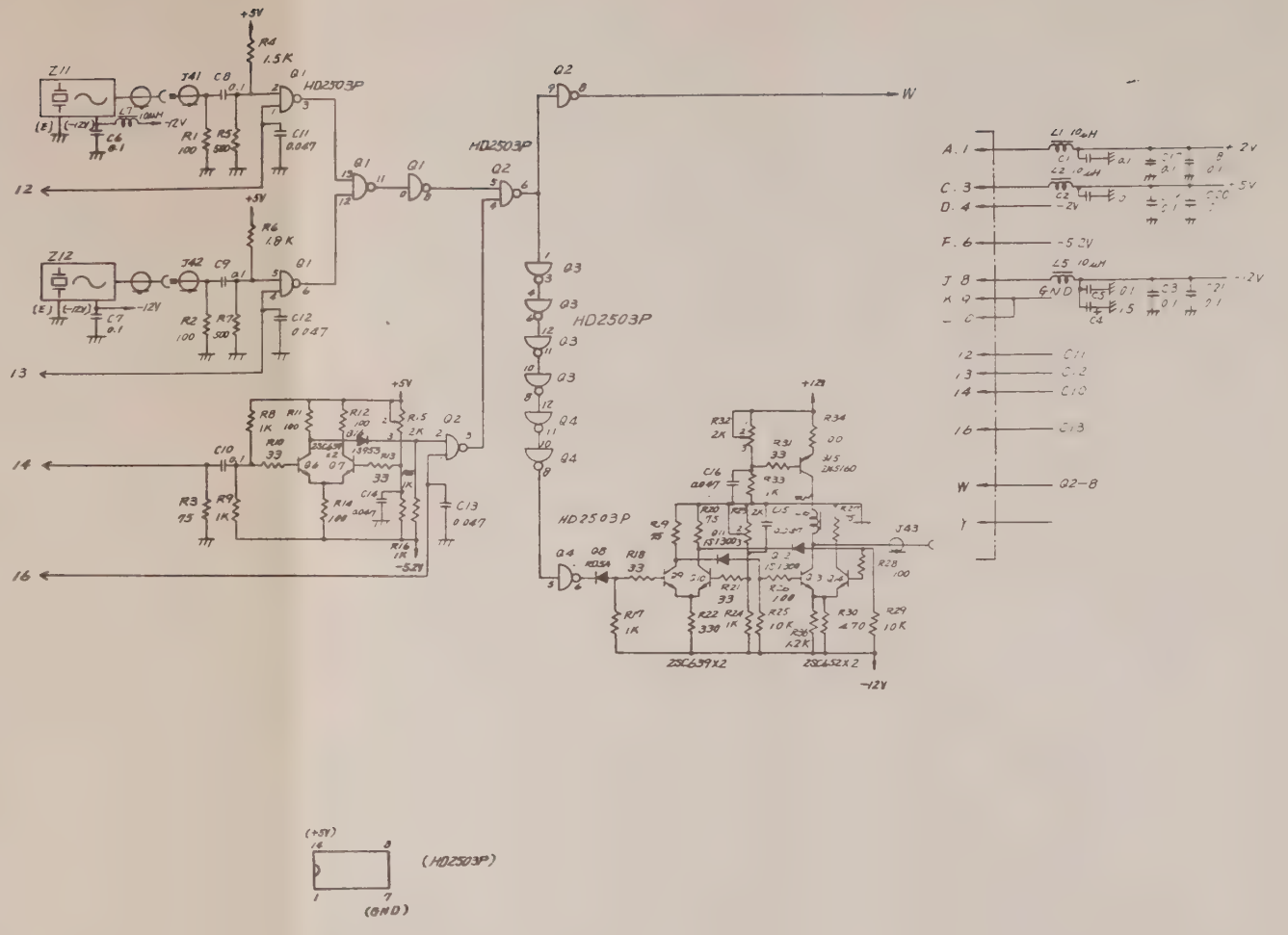
TITLE		
CIRCUIT DIAGRAM OF MOTHER BOARD CIRCUIT (IN ME422A SENDING UNIT)		
SIZE: C	CODE IDENT NO: 12859	DRAWING NO: 48W 3383
SCALE	WEIGHT	SHEET

PARTS LIST TO BE SUPPLIED IN FINAL MANUAL

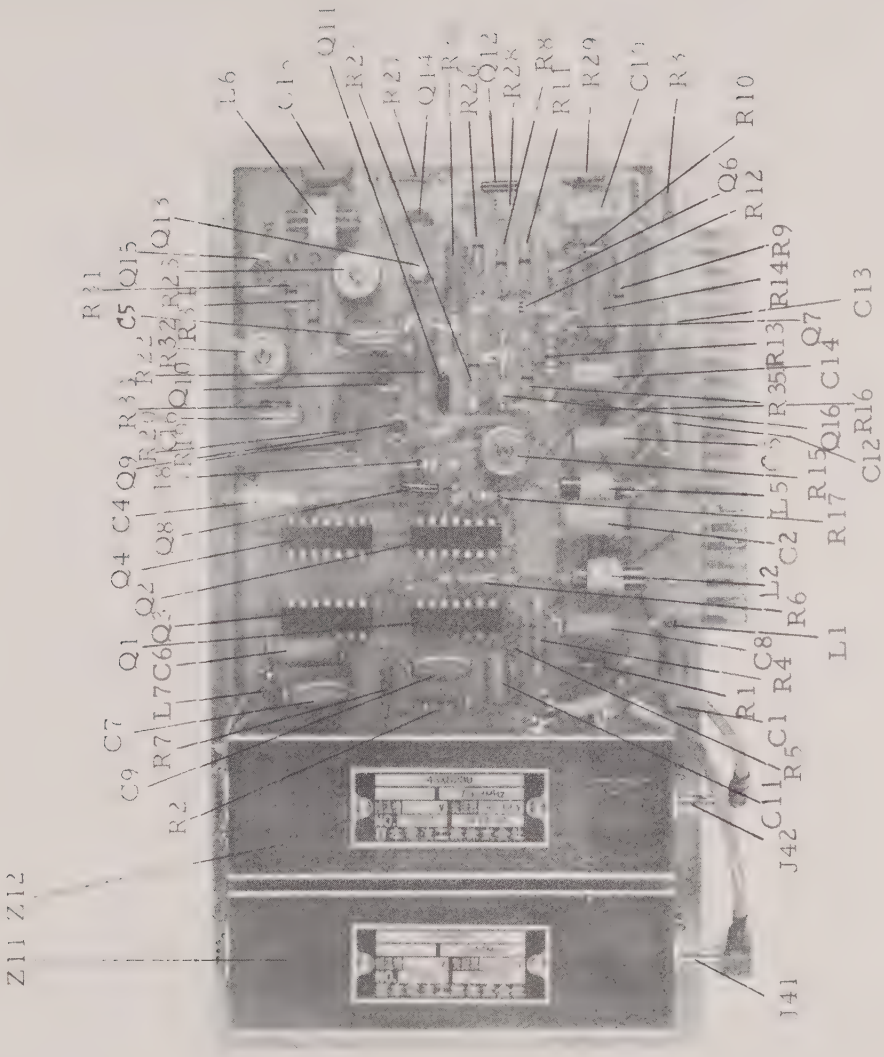
PARTS VALUES LIST

44W42258

REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	0.1μF ±10%, 50V		
C2	0.1μF ±10%, 50V		
C3	0.1μF ±10%, 50V		
C4	15μF +100 -10%, 20V		
C5	0.1μF ±10%, 50V		
C6 to C10	0.1μF ±10%, 50V		
C11 to C16	0.047μF ±10%, 50V		
C17 to C21	0.1μF ±10%, 50V		
L1	10μH		
L2	10μH		
L3	Not assigned		
L4	Not assigned		
L5	10μH		
L6	1mH		
L7	10μH		
R1	100Ω ±5%, 1/8W		
R2	100Ω ±5%, 1/8W		
R3	75Ω ±5%, 1/8W		
R4	1.5kΩ ±5%, 1/8W		
R5	500Ω ±5%, 1/8W		
R6	1.8kΩ ±5%, 1/8W		
R7	500Ω ±5%, 1/8W		
R8	1kΩ ±5%, 1/8W		
R9	1kΩ ±5%, 1/8W		
R10	33Ω ±5%, 1/8W		
R11	100Ω ±5%, 1/8W		
R12	100Ω ±5%, 1/8W		
R13	33Ω ±5%, 1/8W		
R14	100Ω ±5%, 1/2W		
R15	2kΩ		
R16	1kΩ ±5%, 1/8W		
R17	1kΩ ±5%, 1/8W		
R18	33Ω ±5%, 1/8W		
R19	75Ω ±5%, 1/8W		
R20	75Ω ±5%, 1/8W		
R21	33Ω ±5%, 1/8W		
R22	330Ω ±5%, 1/2W		
R23	2kΩ		
R24	1kΩ ±5%, 1/8W		
R25	10kΩ ±5%, 1/8W		
R26	100Ω ±5%, 1/8W		
R27	75Ω ±5%, 1/8W		
R28	100Ω ±5%, 1/8W		
R29	10kΩ ±5%, 1/8W		
R30	470Ω ±5%, 1/2W		
R31	33Ω ±5%, 1/8W		
R32	2kΩ		
R33	1kΩ ±5%, 1/8W		
R34	100Ω ±5%, 1/4W		
R35	1kΩ ±5%, 1/8W		
R36	12.kΩ ±5%, 1/4W		



TITLE		
CIRCUIT DIAGRAM OF CLOCK CIRCUIT (IN ME422A SENDING UNIT)		
SIZE B	CODE IDENT NO. 12859	DRAWING NO. 43W 13793
SCALE	WEIGHT	SHEET

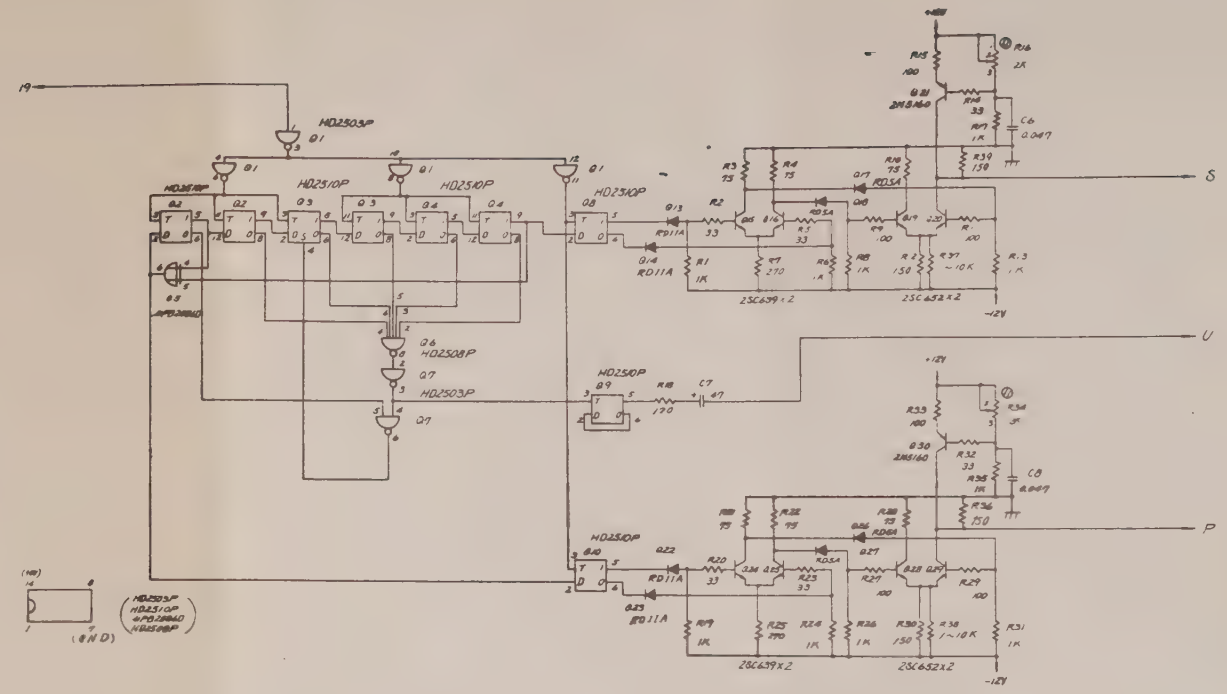


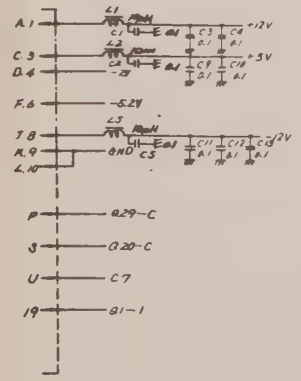
TITLE		
CLOCK CIRCUIT OF 1E422A (Sending unit)		
SIZE A	CODE IDENT NO. 12859	DRAWING NO.
SCALE	WEIGHT	SHEET

PARTS VALUES LIST

44W42259

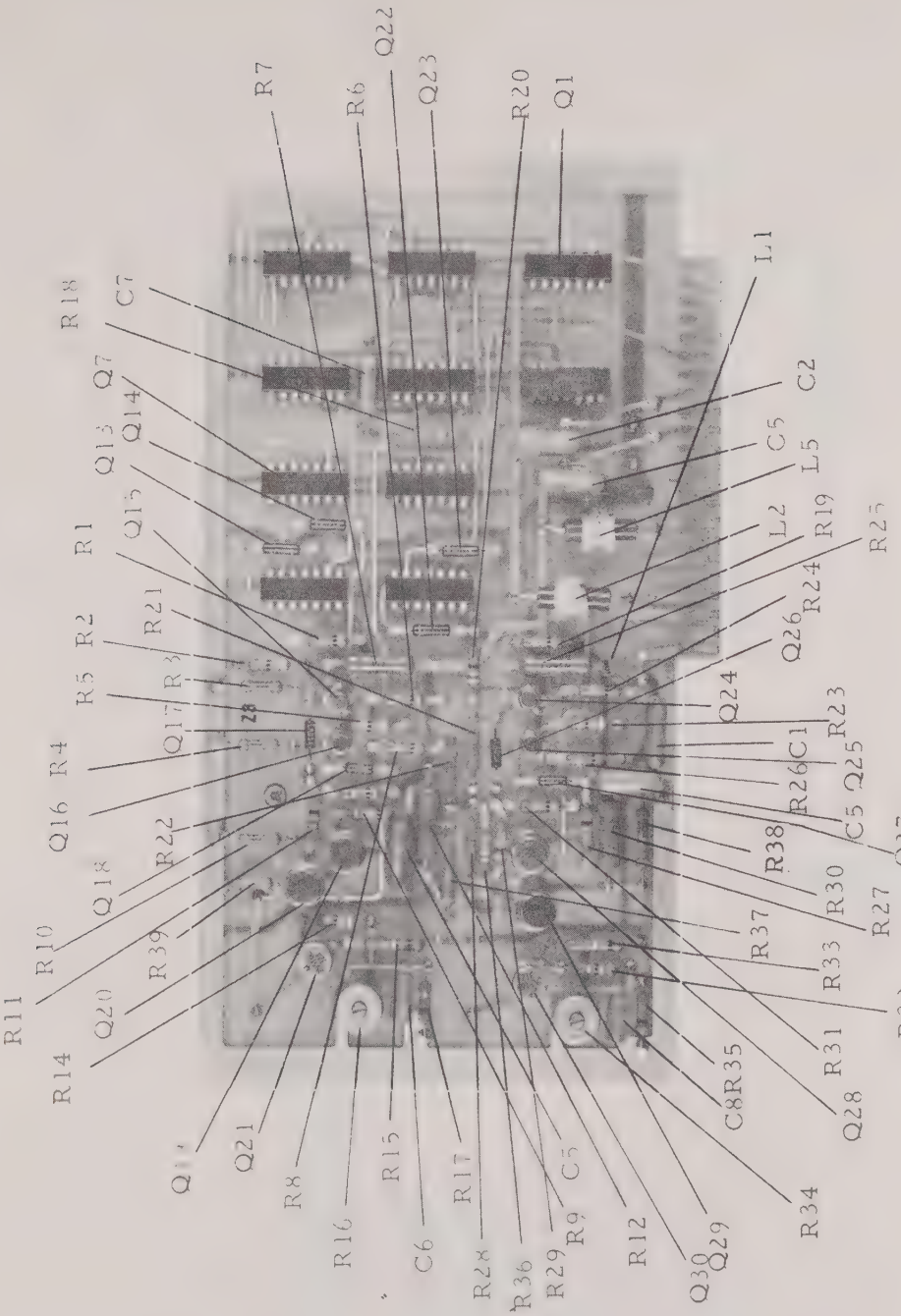
REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1 to C4	0.1μF ±10%, 50V		
C5	0.1μF ±10%, 50V		
C6	0.047μF, 50V		
C7	47μF, ±20%, 6.3V		
C8	0.047μF ±10%, 50V		
C9 to C13	0.1μF ±10%, 50V		
L1	10μH		
L2	10μH		
L3	Not assigned		
L4	Not assigned		
L5	10μH		
R1	1kΩ ±5%, 1/8W		
R2	33Ω ±5%, 1/8W		
R3	75Ω ±5%, 1.8W		
R4	75Ω ±5%, 1/8W		
R5	33Ω ±5%, 1/8W		
R6	1kΩ ±5%, 1/8W		
R7	270Ω ±5%, 1/2W		
R8	1kΩ ±5%, 1/8W		
R9	100Ω ±5%, 1/8W		
R10	75Ω ±5%, 1/8W		
R11	100Ω ±5%, 1/8W		
R12	150Ω ±5%, 1/2W		
R13	1kΩ ±5%, 1/8W		
R14	33Ω ±5%, 1/8W		
R15	100Ω ±5%, 1/4W		
R16	2kΩ		
R17	1kΩ ±5%, 1/8W		
R18	120Ω ±5%, 1/8W		
R19	1kΩ ±5%, 1/8W		
R20	33Ω ±5%, 1/8W		
R21	75Ω ±5%, 1/8W		
R22	75Ω ±5%, 1/8W		
R23	33Ω ±5%, 1/8W		
R24	1kΩ ±5%, 1/8W		
R25	270Ω ±5%, 1/2W		
R26	1kΩ ±5%, 1/8W		
R27	100Ω ±5%, 1/8W		
R28	75Ω ±5%, 1/8W		
R29	100Ω ±5%, 1/8W		
R30	150Ω ±5%, 1/2W		
R31	1kΩ ±5%, 1/8W		
R32	33Ω ±5%, 1/8W		
R33	100Ω ±5%, 1/4W		
R34	2kΩ		
R35	1kΩ ±5%, 1/8W		
R36	150Ω ±5%, 1/8W		
R37	1 to 10kΩ ±5%, 1/4W		
R38	1 to 10kΩ ±5%, 1/4W		
R39	150Ω ±5%, 1/8W		



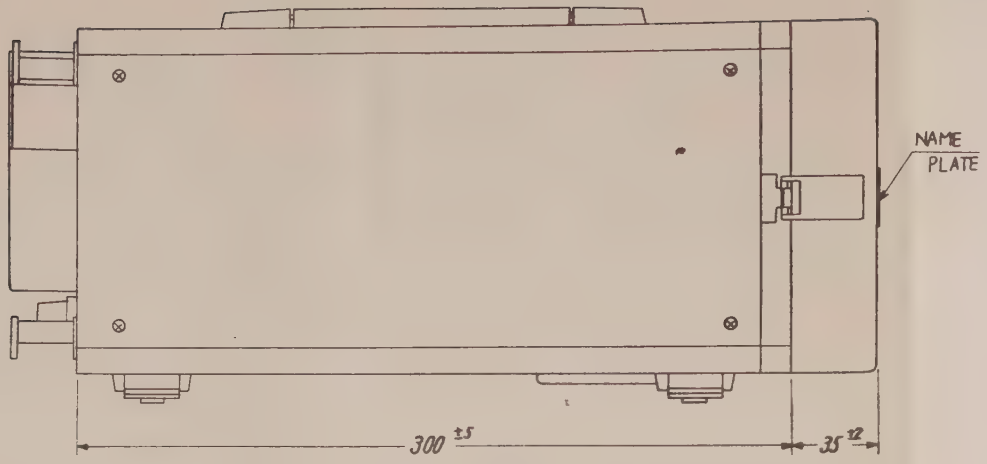


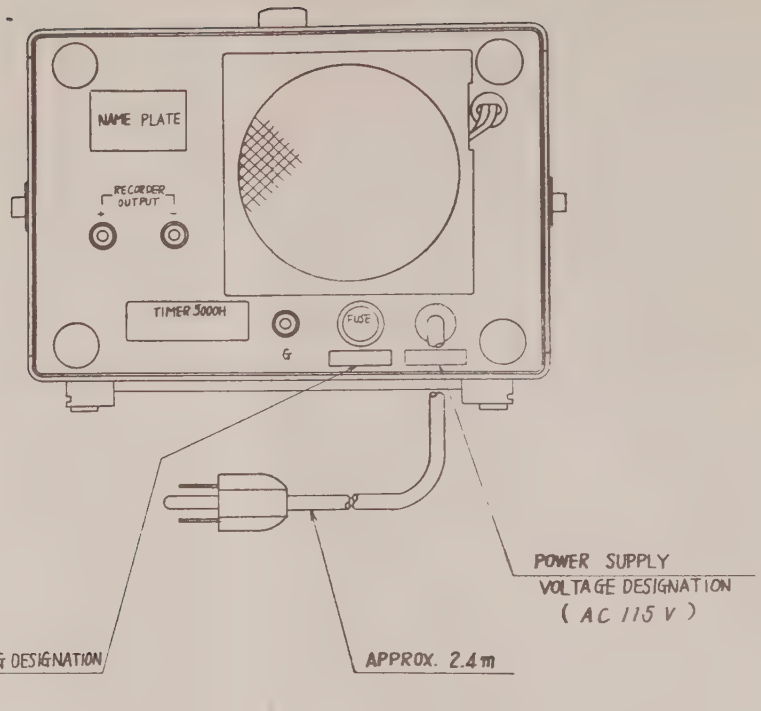
TITLE: CIRCUIT DIAGRAM OF PATTERN GENERATOR CIRCUIT (IN ME422A SENDING UNIT)		
SIZE: C	CODE IDENT NO: 12859	DRAWING NO: 48W 3384
SCALE	WEIGHT	SHEET

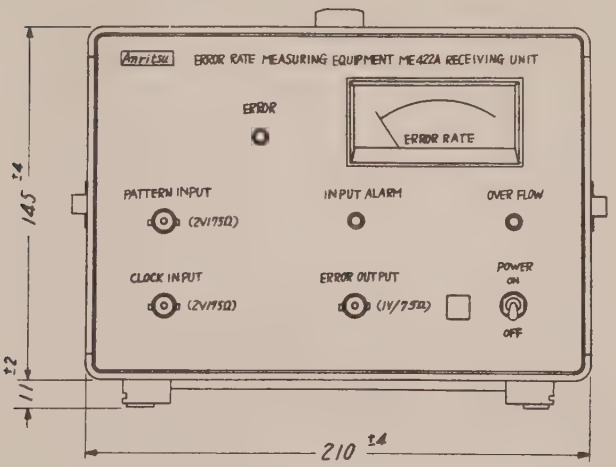
PARTS LIST TO BE SUPPLIED IN FINAL MANUAL



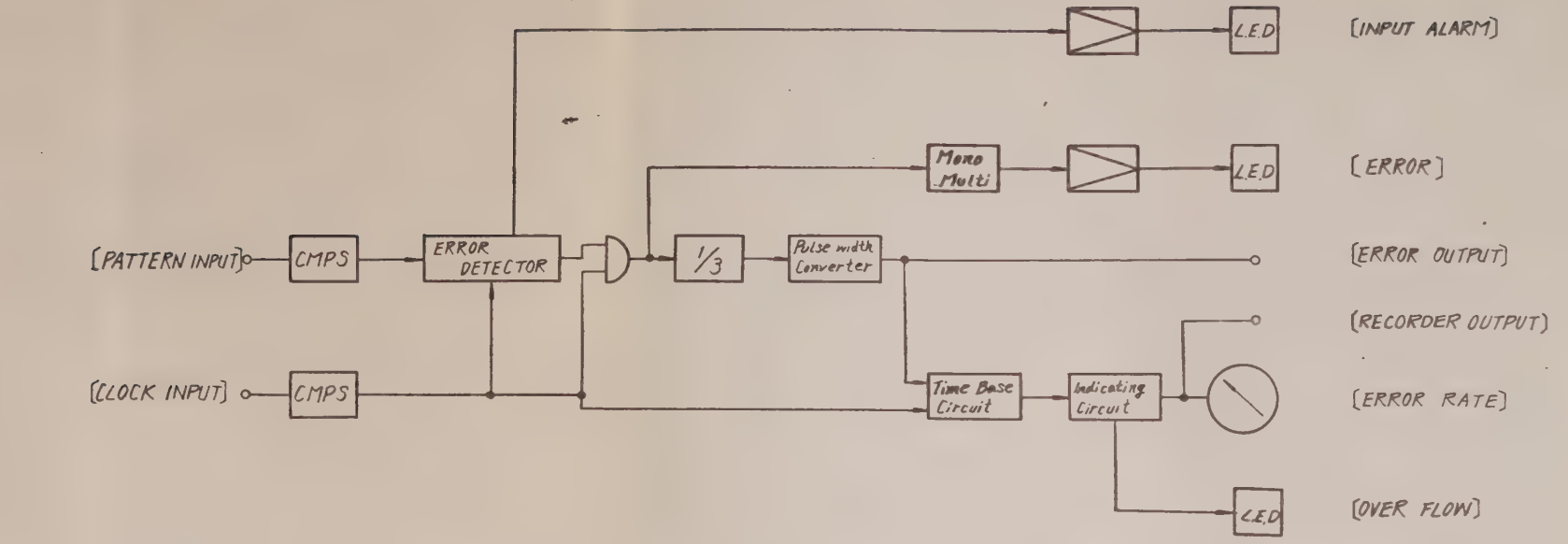
TITLE		
PATTERN GENERATING & OUTPUT-CH1. CH2 CIRCUIT OF ME422A (Sending unit)		
SIZE	CODE IDENT NO.	DRAWING NO.
A	12859	3-008
SCALE	WEIGHT	SHEET



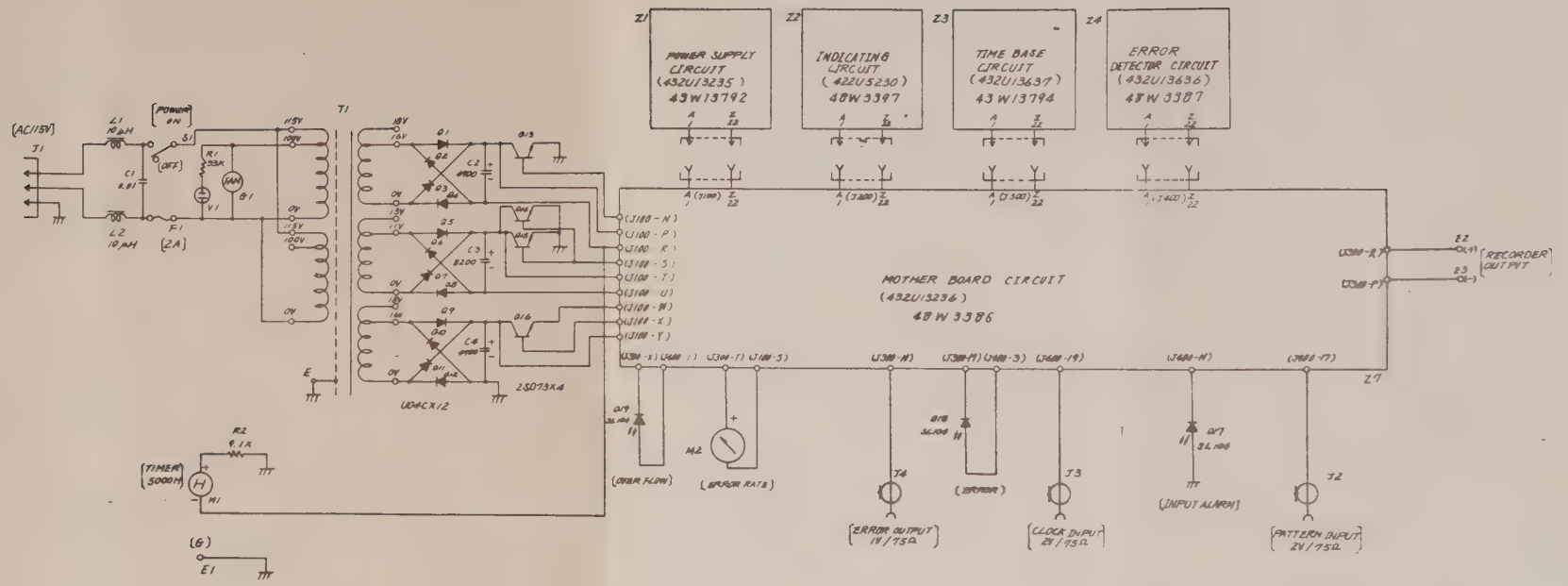




TITLE		
FRONT VIEW AND OTHER VIEWS OF ERROR RATE MEASURING EQUIPMENT ME422A RECEIVING UNIT.		
SIZE: C	CODE IDENT NO.: 12859	DRAWING NO.: 49W 1889
SCALE	WEIGHT	SHEET



TITLE: BLOCK DIAGRAM OF ME422A RECEIVING UNIT		
SIZE: B	CODE IDENT NO.: 12859	DRAWING NO.: 43W13905
SCALE	WEIGHT	SHEET



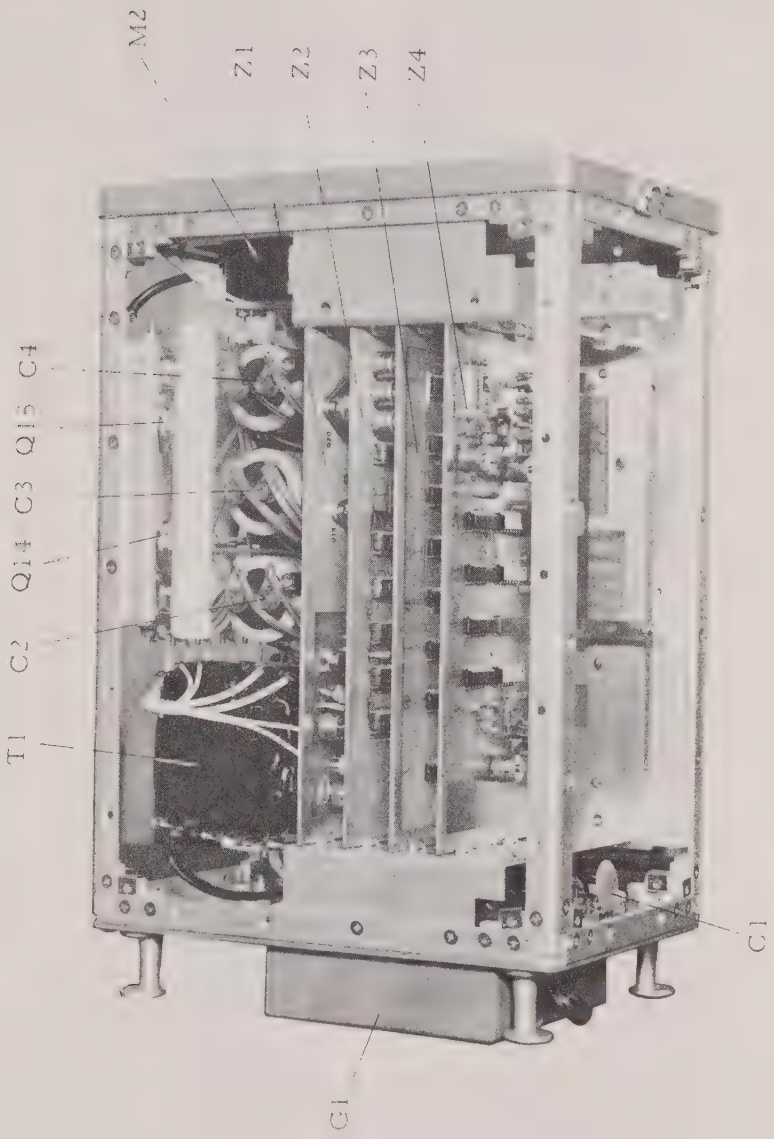
PARTS VALUES LIST

44W42260

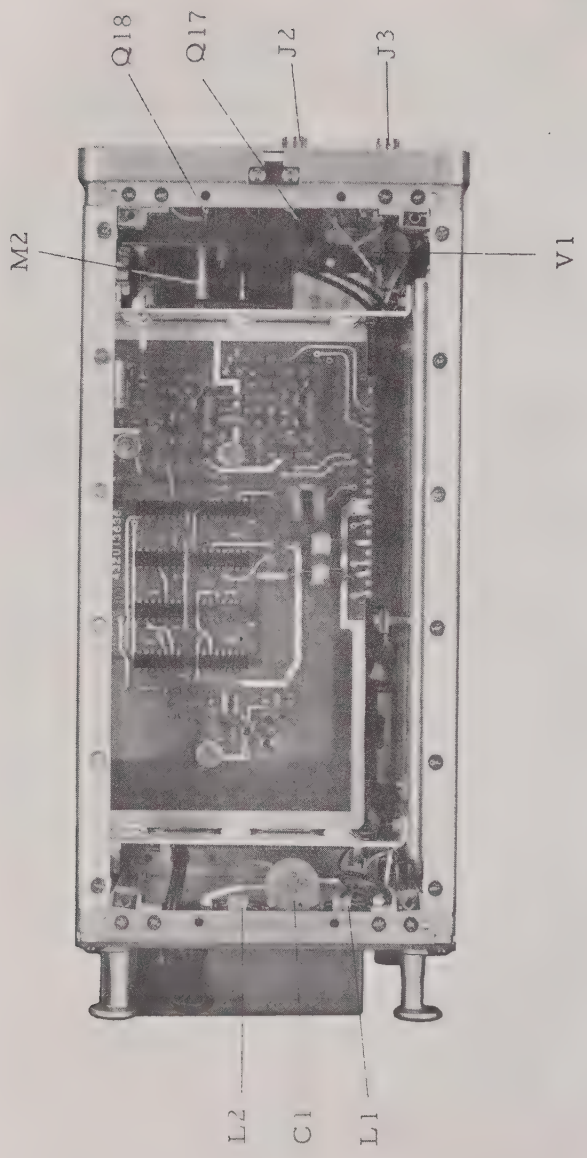
REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	10000pF +80 -20%, 50V		
C2	4700pF +50 -10%, 35V		
C3	8200μF +50 -10%, 25V		
C4	4700μF +50 -10%, 35V		
L1	10μH		
L2	10μH		
R1	33kΩ ±5%, 1/4W		
R2	9.1kΩ ±5%, 1/4W		

TITLE		
CIRCUIT DIAGRAM OF ERROR RATE MEASURING EQUIPMENT ME422A RECEIVING UNIT		
SIZE: C	CODE IDENT NO.: 12859	DRAWING NO: 48W3385
SCALE	WEIGHT: —	SHEET

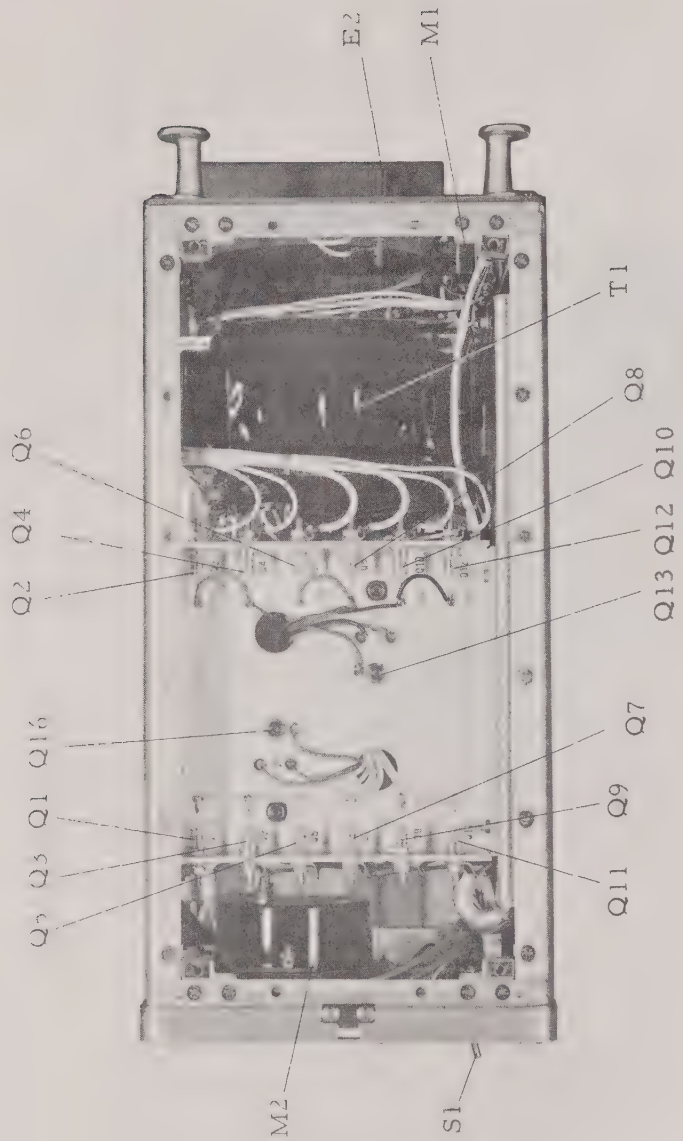
PARTS LIST TO BE SUPPLIED IN FINAL MANUAL



TITLE		
ME422A (RECEIVING UNIT		
SIZE: A	CODE IDENT NO.: 12859	DRAWING NO.: 4-006
SCALE	WEIGHT	SHEET



TITLE		
ME422A (RECEIVING UNIT)		
SIZE A	CODE IDENT NO. 12859	DRAWING NO. 4-006
SCALE	WEIGHT	SHEET 2 3

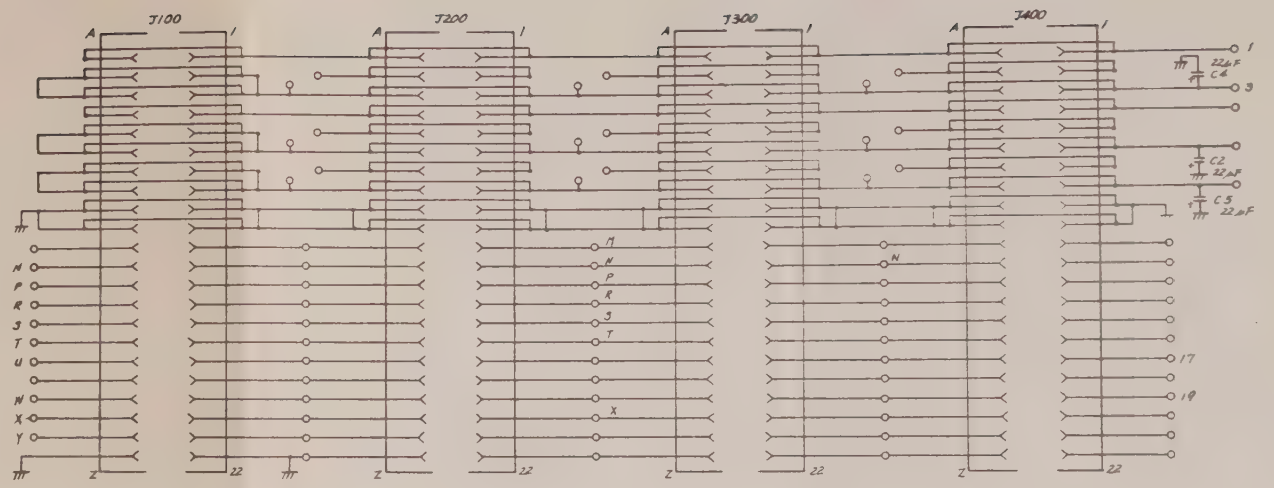


TITLE		
ME422A (RECEIVING UNIT)		
SIZE A	CODE IDENT NO. 12859	DRAWING NO
SCALE	WEIGHT	SHEET

PARTS VALUES LIST

44842261

REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	Not assigned		
C2	22μF +100 -10%, 16V		
C3	Not assigned		
C4, C5	22μF +100 -10%, 16V		

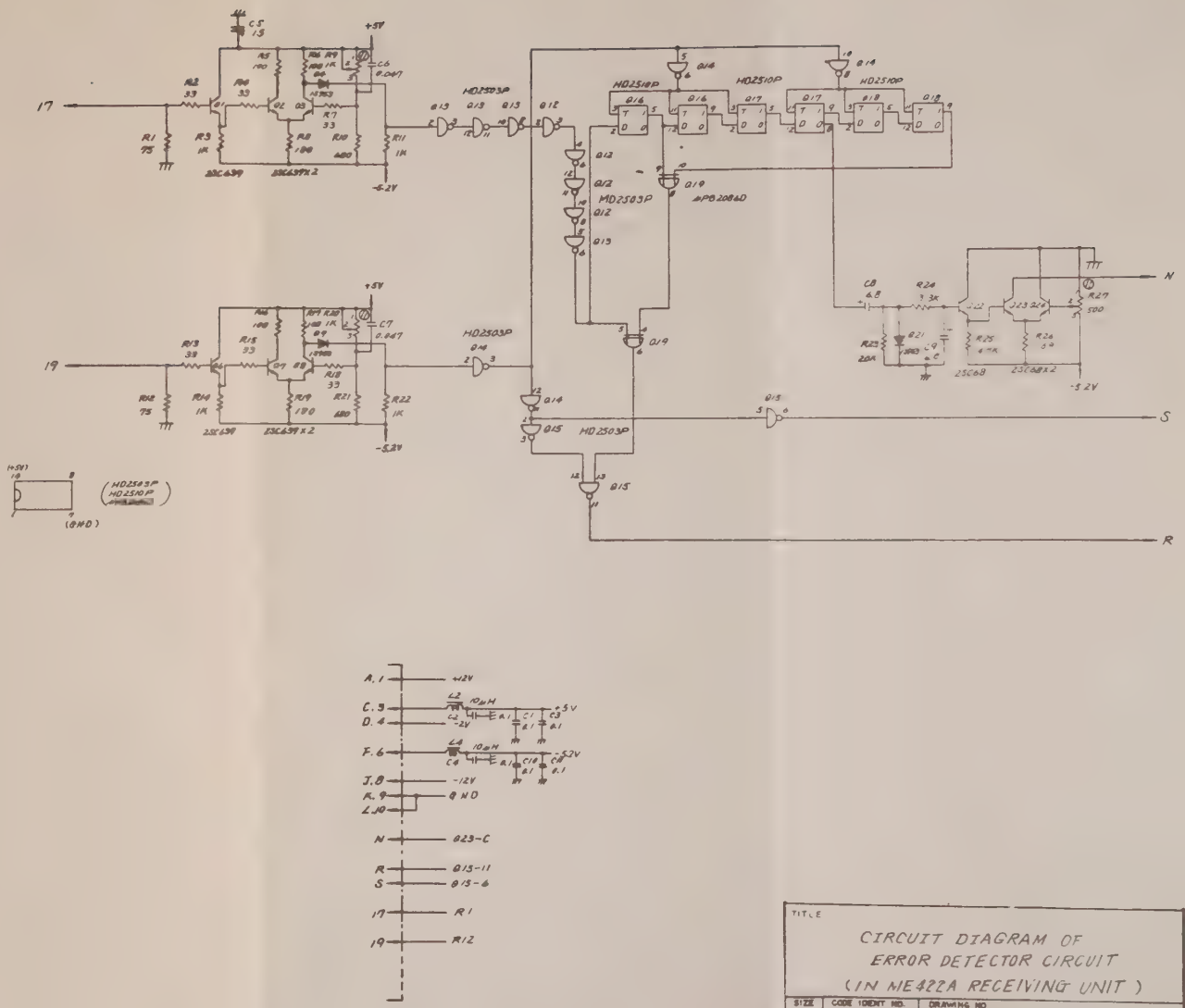


TITLE		
CIRCUIT DIAGRAM OF MOTHER BOARD CIRCUIT (IN ME422A RECEIVING UNIT)		
SIZE: C	CODE IDENT NO: 12859	DRAWING NO: 48W 3386
SCALE	WEIGHT	SHEET

PARTS LIST TO BE SUPPLIED IN FINAL MANUAL

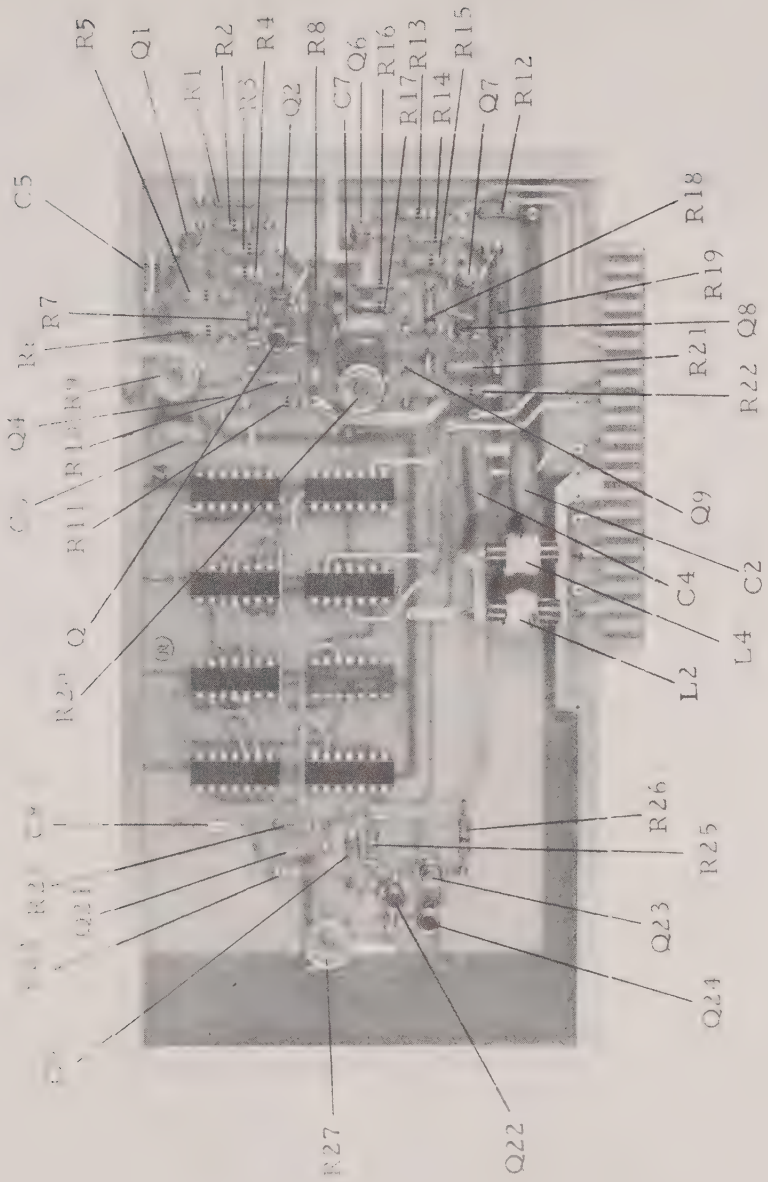
PARTS VALUES LIST 44W42262

REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1 to C4	0.1μF ±10%, 50V		
C5	15μF +100 -10%, 20V		
C6	0.047μF ±10%, 50V		
C7	0.047μF ±10%, 50V		
C8	6.8μF ±20%, 6.3V		
C9	6.8μF ±20%, 6.3V		
C10 to C11	0.1μF ±10%, 50V		
L1	Not assigned		
L2	10μH		
L3	Not assigned		
L4	10μH		
R1	75Ω ±5%, 1/8W		
R2	33Ω ±5%, 1/8W		
R3	1kΩ ±5%, 1/8W		
R4	33Ω ±5%, 1/8W		
R5	100Ω ±5%, 1/8W		
R6	100Ω ±5%, 1/8W		
R7	33Ω ±5%, 1/8W		
R8	180Ω ±5%, 1/2W		
R9	1kΩ		
R10	680Ω ±5%, 1/8W		
R11	1kΩ ±5%, 1/8W		
R12	75Ω ±5%, 1/8W		
R13	33Ω ±5%, 1/8W		
R14	1kΩ ±5%, 1/8W		
R15	33Ω ±5%, 1/8W		
R16	100Ω ±5%, 1/8W		
R17	100Ω ±5%, 1/8W		
R18	33Ω ±5%, 1/8W		
R19	180Ω ±5%, 1/2W		
R20	1kΩ		
R21	680Ω ±5%, 1/8W		
R22	1kΩ ±5%, 1/8W		
R23	20kΩ ±5%, 1/8W		
R24	3.3kΩ ±5%, 1/8W		
R25	4.7kΩ ±5%, 1/8W		
R26	68Ω ±5%, 1/8W		
R27	500Ω		



TITLE	CIRCUIT DIAGRAM OF ERROR DETECTOR CIRCUIT (IN ME422A RECEIVING UNIT)
SIZE: C	CODE IDENT NO.: 12859
DRAWING NO:	48W 3387
SCALE	WEIGHT
SHEET	

PARTS LIST TO BE SUPPLIED IN FINAL MANUAL

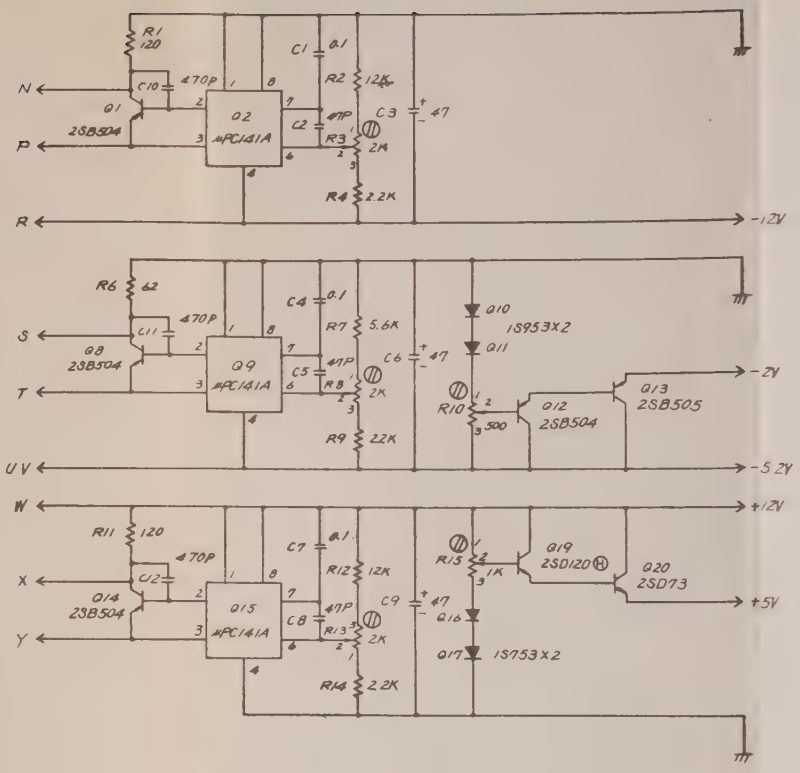


TITLE		
ERROR DETECTING CIRCUIT OF ME422A (Receiving unit)		
SIZE: A	CODE IDENT NO.: 12859	DRAWING NO: 3-017
SCALE	WEIGHT	SHEET

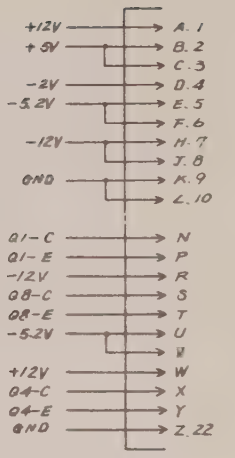
PARTS VALUES LIST

44W4225T

REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	0.1μF ±10%, 50V		
C2	47pF ±5%, 50V		
C3	47μF +100 -10%, 25V		
C4	0.1μF ±10%, 50V		
C5	47pF ±5%, 50V		
C6	47μF +100 -10%, 25V		
C7	0.1μF ±10%, 50V		
C8	47pF ±5%, 50V		
C9	47μF +100 -10%, 25V		
C10 to C12	470pF ±5%, 50V		
R1	120Ω ±5%, 1/8W		
R2	12kΩ ±5%, 1/8W		
R3	2kΩ		
R4	2.2kΩ ±5%, 1/8W		
R5	Not assigned		
R6	62Ω ±5%, 1/8W		
R7	5.6kΩ ±5%, 1/8W		
R8	2kΩ		
R9	2.2kΩ ±5%, 1/8W		
R10	500Ω		
R11	120Ω ±5%, 1/8W		
R12	12kΩ ±5%, 1/8W		
R13	2kΩ		
R14	2.2kΩ ±5%, 1/8W		
R15	1kΩ		

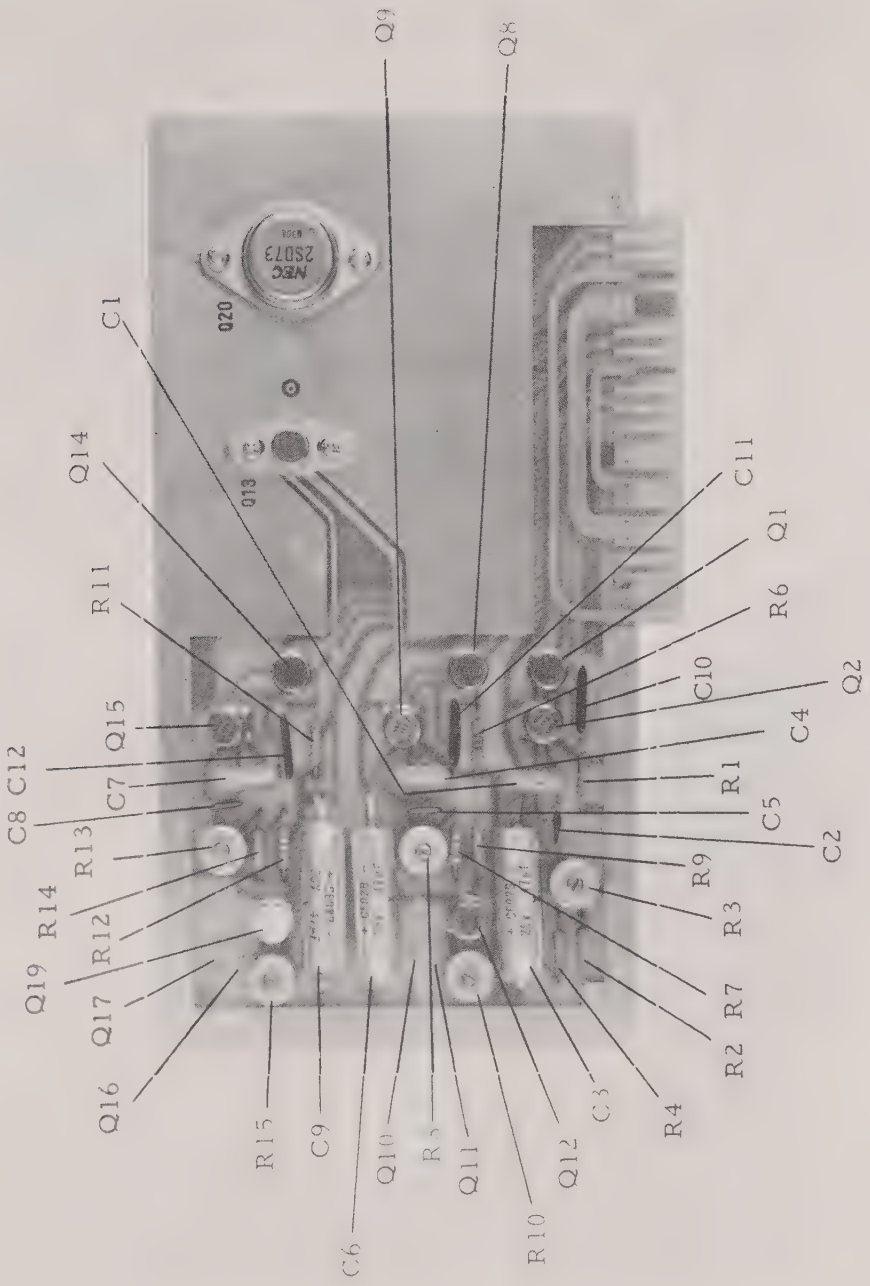


(μPC141A)



TITLE	CIRCUIT DIAGRAM OF POWER SOURCE CIRCUIT (IN ME422A SENDING/RECEIVING UNITS)	
SIZE B	CODE IDENT NO. 12859	DRAWING NO. 43W 13792
SCALE	WEIGHT	SHEET

PARTS LIST TO BE SUPPLIED IN FINAL MANUAL

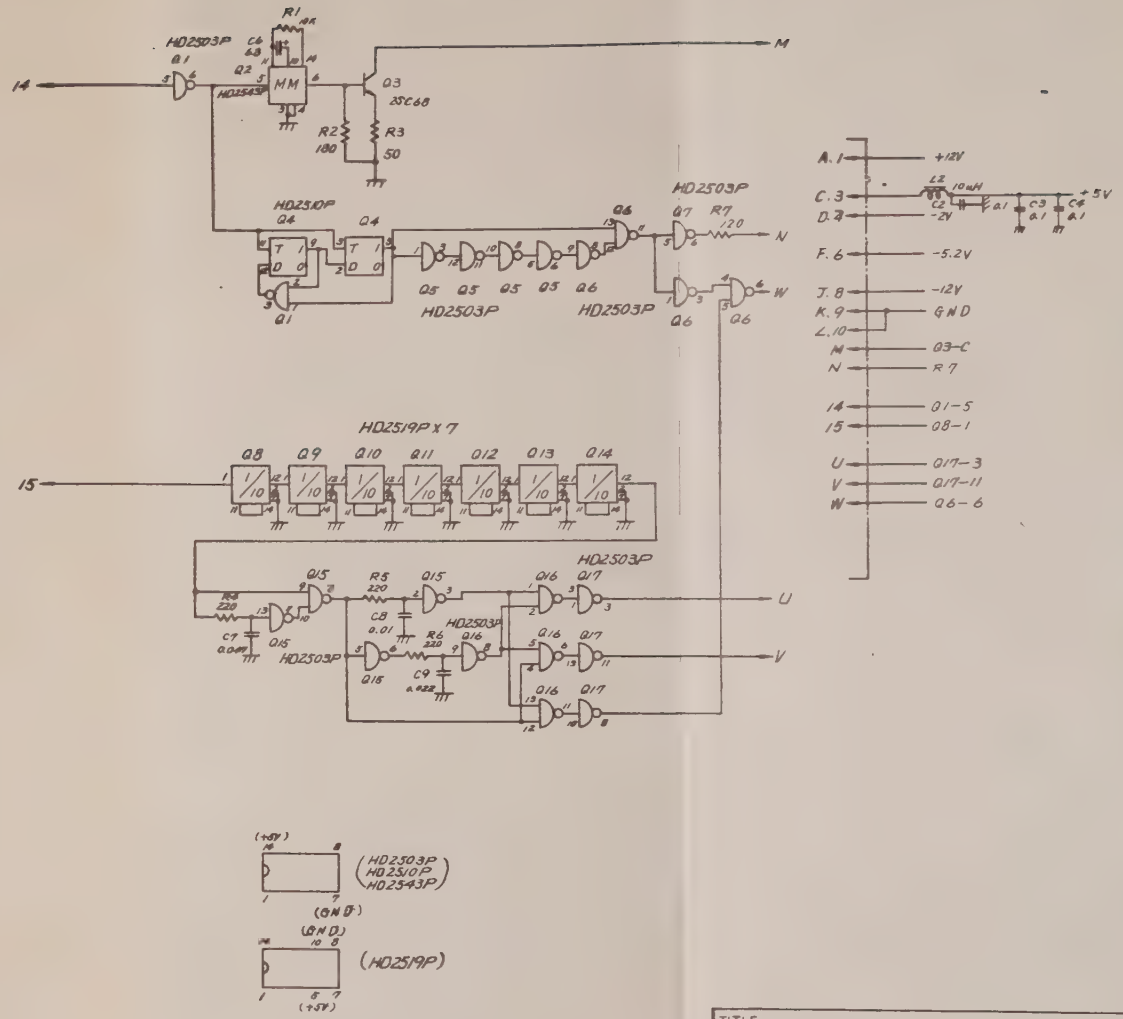


TITLE		
DC POWER SOURCE CIRCUIT OF ME 422A		
SIZE A	CODE IDENT NO 12859	DRAWING NO
SCALE	WEIGHT	SHEET

PARTS VALUES LIST

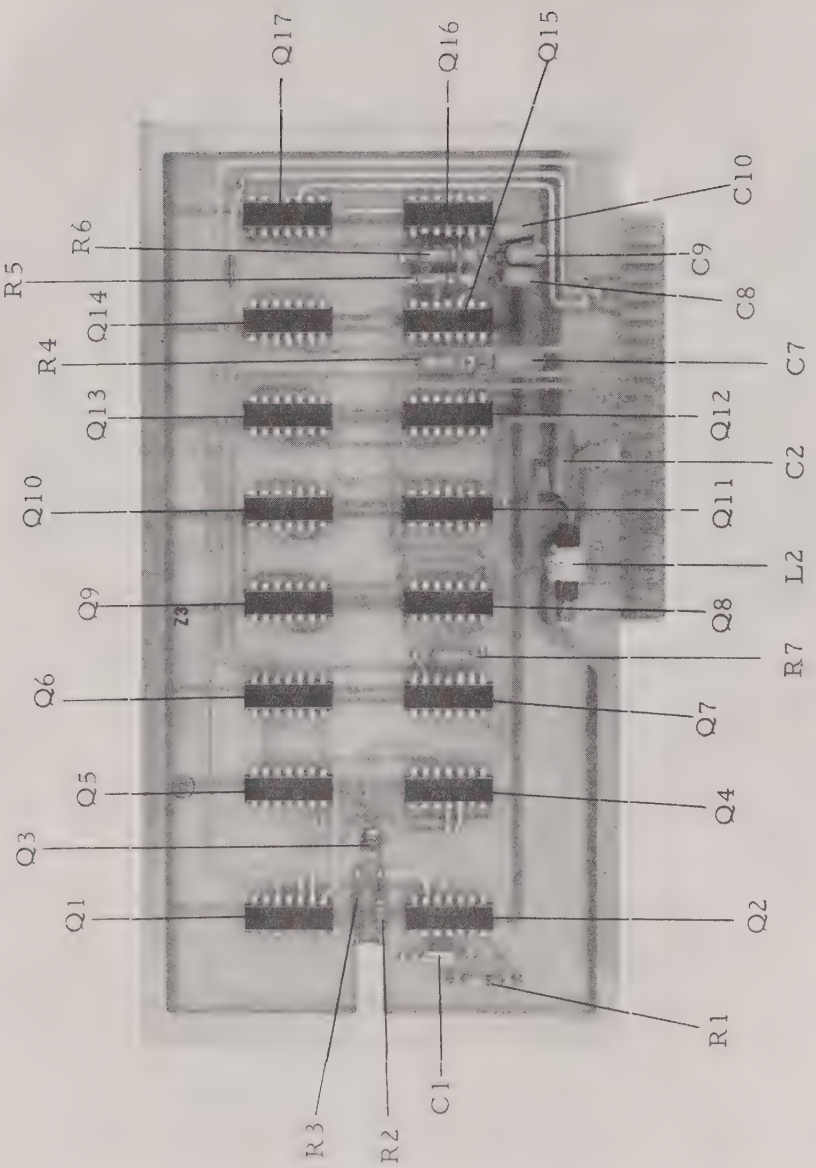
44W42263

REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	Not assigned		
C2	0.1μF ±10%, 50V		
C3 to C4	0.1μF ±10%, 50V		
C6	6.8μF ±20%, 6.3V		
C7	0.047μF ±10%, 50V		
C8	0.01μF ±10%, 50V		
C9	0.022μF ±10%, 50V		
L1	Not assigned		
L2	10μH		
R1	10kΩ ±5%, 1/8W		
R2	180Ω ±5%, 1/8W		
R3	50Ω ±5%, 1/8W		
R4 to R6	220Ω ±5%, 1/8W		
R7	120Ω ±5%, 1/8W		

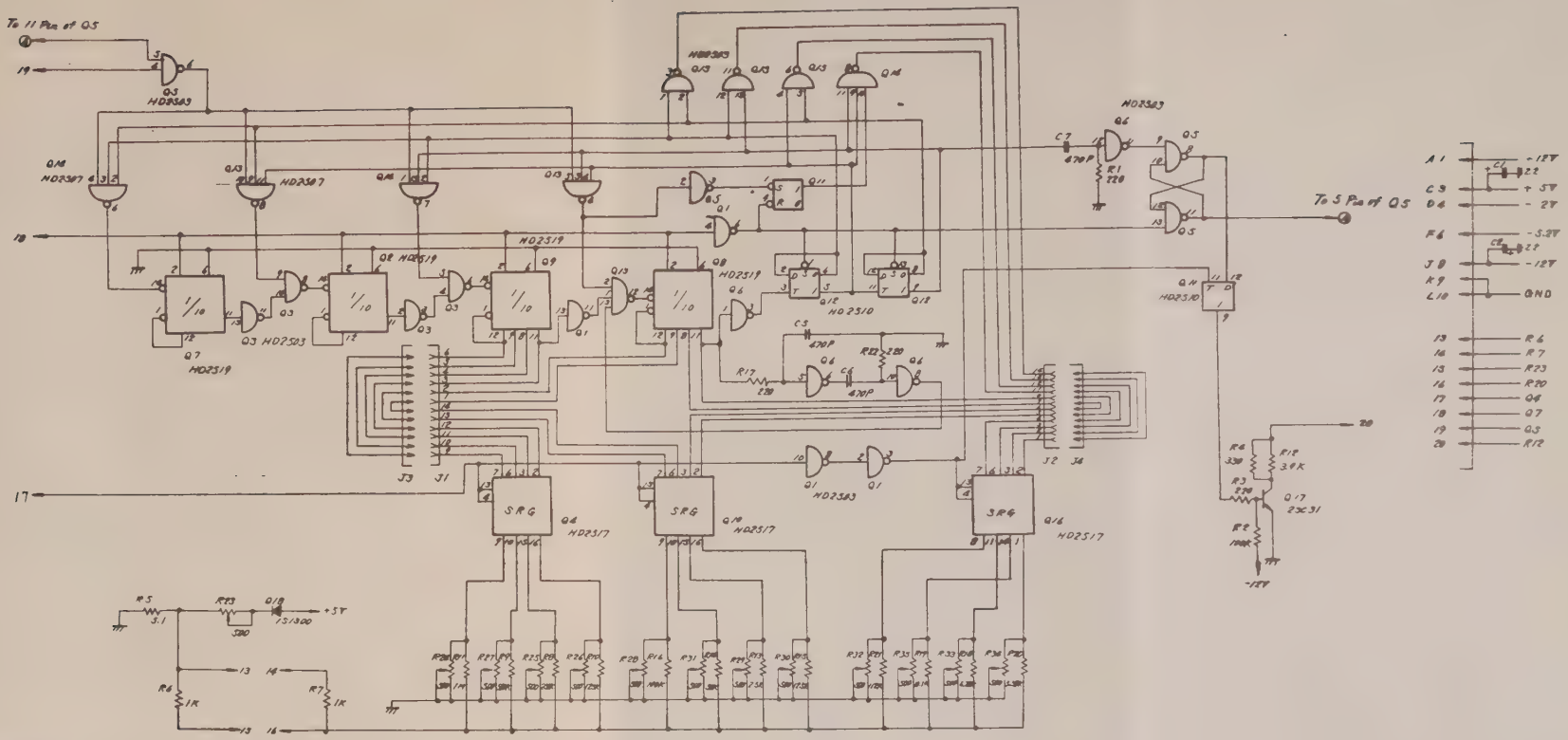


TITLE	CIRCUIT DIAGRAM OF TIME BASE CIRCUIT (IN ME422A RECEIVING UNIT)	
SIZE B	CODE IDENT NO. 12859	DRAWING NO. 43W 13794
SCALE	WEIGHT	SHEET

PARTS LIST TO BE PROVIDED IN FINAL MANUAL



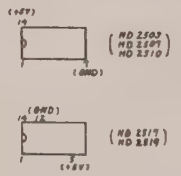
TITLE		
TIME BASE PULSE GENERATING CIRCUIT OF ME422A (Receiving unit)		
SIZE	CODE IDENT NO.	DRAWING NO.
A	12859	3-007
SCALE	WEIGHT	SHEET



PARTS VALUES LIST

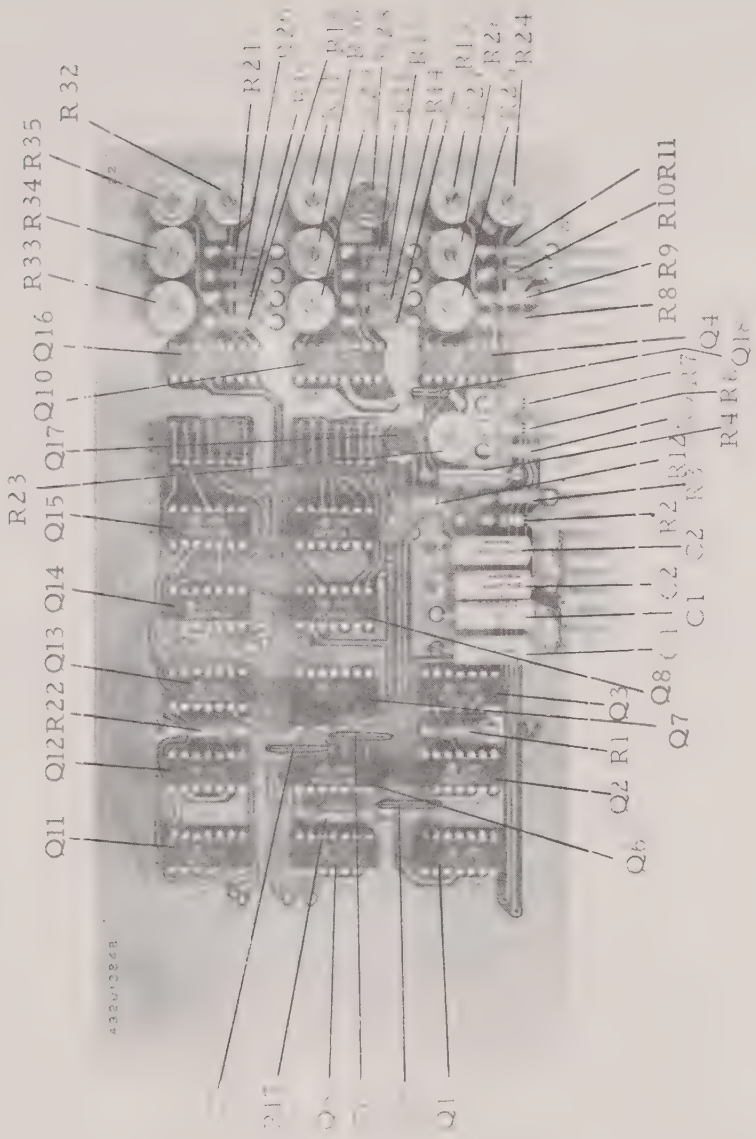
44W42264

REFERENCE DESIGNATORS	RATING	REFERENCE DESIGNATORS	RATING
C1	2.2μF +150 -10%, 63V		
C2	2.2μF +150 -10%, 63V		
C3	Not assigned		
C4	Not assigned		
C5 to C7	470pF ±5%, 50V		
R1	220Ω ±5%, 1/8W		
R2	100kΩ ±5%, 1/8W		
R3	220Ω ±5%, 1/8W		
R4	330Ω ±5%, 1/2W		
R5	5.1Ω ±5%, 1/8W		
R6	1kΩ ±5%, 1/8W		
R7	1kΩ ±5%, 1/8W		
R8	250Ω ±0.5%, 1/8W		
R9	500kΩ ±0.5%, 1/8W		
R10	125kΩ ±0.5%, 1/8W		
R11	1MΩ ±0.5%, 1/8W		
R12	3.9kΩ ±5%, 1/8W		
R13	25kΩ ±0.5%, 1/8W		
R14	50kΩ ±0.5%, 1/8W		
R15	12.5kΩ ±0.5%, 1/8W		
R16	100kΩ ±0.5%, 1/8W		
R17	220Ω ±5%, 1/8W		
R18	5.28kΩ ±0.5%, 1/8W		
R19	10.1kΩ ±0.5%, 1/8W		
R20	3.58kΩ ±0.5%, 1/8W		
R21	112kΩ ±0.5%, 1/8W		
R22	220Ω ±5%, 1/8W		
R23 to R35	500Ω		



TITLE		
CIRCUIT DIAGRAM OF INDICATNG CIRCUIT (IN ME422A RECEIVING UNIT)		
SIZE	CODE IDENT NO	DRAWING NO
C	12859	48W3397
SCALE	WEIGHT	SHEET 1

PARTS LIST TO BE SUPPLIED IN FINAL MANUAL



TITLE		
SIZE A	CODE IDENT NO	DRAWING NO
SCALE	WEIGHT	SHEET

SUPPLEMENT
FOR
INSTRUCTION MANUAL
OF
ME422A ERROR RATE MEASURING EQUIPMENT

General

Pulse generator circuit of transmitting unit has some parts selected at test (SAT).

Following is the selecting procedure of SAT.

1. ME422A ERROR RATE MEASURING EQUIPMENT

Transmitting Unit, Pulse Generator Circuit.

1.1 List of SAT

SYMBOL	STANDARD VALUE	ADJUSTING RANGE
R37 and R38	5.1 kΩ	1 - 10 kΩ

1.2 Test Equipment Required

Pulse Generator	8002A (HP)
Oscilloscope	485A (Tektronix)

Equivalent test equipment may be used.

1.3 Procedure

Step	Procedure
1.	Output 1
1.1	Apply a signal from 8002A Pulse Generator (3 Vo-p/50Ω, duty factor 50%, 10 MHz) to terminal 19.
1.2	Observe waveform of terminal P on 485A Oscilloscope. Vary value of resistor R38 so that output level becomes 2V.
2.	Output 2
2.1	Apply signal as in 1.1 above.
2.2	Observe waveform of terminal S. Vary value of resistor R37 so that output level becomes 2V.

MP MASTER
MA35820